IBM Field Engineering

Maintenance Manual

1130 Computing System

SY26-5977-5

Preface

This manual contains all maintenance procedures required to service the IBM 1130 Computing System.

This manual assumes that the CE has limited experience and/or training on the system and is familiar with the material contained in the Field Engineering Theory of Operation manuals listed in this preface.

Wiring diagrams (logics) at the engineering change level of the specific machine are included in each machine shipment.

The 1131 Models 4A and 4B and the 1132 Model 2 are available only in the United States and Canada.

Sixth Edition (November 1972)

This is a reprint of SY26-5977-4 incorporating changes released in Technical Newsletters SN34-0044 and SN34-0070, dated August 1971 and May 1972.

Specifications contained herein are subject to change. Changes will be reported in subsequent revisions of Technical Newsletters (TNL's).

Some illustrations in this manual have a code number in the lower corner. This is a publishing control number and is not related to the subject matter.

Requests for copies of this and other IBM publications should be made to your IBM representative or the IBM office serving your locality.

A form for readers' comments is provided at the back of this publication. If the form has been removed, send your comments to IBM Corporation, Systems Publications, Department 27T, P. O. Box 1328, Boca Raton, Florida, 33432. Comments become the property of IBM.

Field Engineering Manuals

Subject	*Type*	*Order No.*
1130 Computing System Includes: 1131 Central Processing Unit 3.6 μs Core Storage 2.2 μs Core Storage Disk Storage (single disk) 115 vac 60 Hz Power 208 vac 60 Hz Power	FE Theory of Operation	SY26-5978
1130 Computing System – Features Includes: 1132 Printer Adapter 1134/1055 Paper Tape Reader-Punch Adapter 1231 Optical Mark Page Reader Adapter 1442 Models 5, 6, and 7 Card Read Punch Adapter 1627 Models 1 and 2 Plotter Adapter 2501 Card Reader Adapter Synchronous Communications Adapter Storage Access Channel Adapter	FE Theory of Operation	SY26-3670
1133 Multiplexer Control Includes: Storage Access Channel 2 Adapter 2310 B Models 1 and 2 Disk Storage Adapter 2311 Models 11 and 12 Disk Storage Adapter 1403 Models 6 and 7 Printer Adapter	FE Theory-Maintenance	SY26-4014
1133 Multiplexer Control Includes: 1133 Multiplexer Control 2310 B Disk Storage Adapter 1403 Printer Adapter	FE Maintenance Diagrams	SY26-4136
Selectric I/O Keyboardless Printer	FE Theory of Operation FE Maintenance Manual	S225-3353 S225-3207
Single Disk Storage (Incremental Access) 2311 Disk Storage Drive, Models 1, 11, and 12	FE Theory of Operation FE Maintenance Manual FE Theory of Operation FE Maintenance Manual	SY26-3669 SY26-3668 SY26-5897 SY26-5923

In addition to the manuals in the foregoing list, theory-of-operation manuals and maintenance manuals are available for the I/O units that can be attached to the 1130 system. Order numbers for these manuals can be found in the IBM Maintenance Library *KWIC Index*, GY20-0073, available in the branch office library.

Unpacking/packing Instructions

Machine Type	*Document Part Number*
1131 CPU	7351131
1131 Memory Addition	7374605

Contents

DANGERS

Personal safety cannot be overemphasized. To ensure your own safety and the safety of co-workers, make it an everyday practice to follow safety precautions at all times. Become familiar with and use the safety practices outlined in the pocket-size card, IBM Form 229-1264-1, issued to all Customer Engineers.

Voltages

Potential difference within the electronic gates, printed cards, and display back panel is +48 vdc to -3 vdc. Do not remove or replace circuit cards when dc power is on. Do not short out or bypass safety features.

Power Supplies

Extreme care must be exercised when servicing or inspecting the power supply even though the voltage range on the machine is low. Dangerous voltages and currents are present even when the system is in a power-off status. If it is necessary to connect a test instrument within the power supply, or to reach into it for any reason, disconnect the mainline cord. Discharge capacitors before working near them. Each heat sink is at an electrical potential. Do not short heat sinks to each other or to the machine frame.

Grounding

Convenience outlets for Customer Engineers are provided in the 1131, 1132, 1133, 2501, 2310B, 2311, 1403, and 1442.

Machine grounding is required. Three-wire grounded power cords are provided. The third wire is for grounding and must not carry current from any source. It is important to the safety of personnel that if any machine of a group is grounded, all other equipment of the group must be grounded. Grounded machines must be placed so that it is not possible for a person to touch both a grounded machine and any ungrounded metal equipment. Grounded machines do not present a hazard in themselves; the real hazard is from ungrounded electrical equipment.

Console Printer (Modified IBM SELECTRIC ®)

Working in certain areas of the typewriter is particularly hazardous because of the positive action of the typewriter. Follow safe working practices. Because it is not possible to foresee each individual area of exposure, the following general rules serve as a guide when working on this equipment.

1. At the completion of a service call, replace gear guards and dust shields. These safety guards are installed to prevent the operator from placing his hands too near moving parts. Because most operators do not have a complete knowledge of the mechanical workings of the machine, the only way to protect them adequately is to place guards over the exposed areas. Be cautious when servicing this machine during the time the rear guards and dust shields are removed.
2. When lubricating, replacing parts, etc., make sure the machine is turned off. It is a good idea to remove the motor plug from the socket after turning the switch to the off position.
3. Exercise caution when handling the motor. The shaded-pole motor used in this machine runs considerably hotter than the capacitor type motor used in the Model B typewriter.
4. Be particularly careful to avoid injury to the hands from sharp edges on stamped parts, springs, links, etc., when picking up and handling all types of machines. Although the safety of the operator and the CE is one of the prime considerations in the design of the product, mass production techniques do not permit separate operations on each part to provide a smooth edge.
5. Wear safety glasses when performing any work that could result in parts, lubricants, cleaning solvents, or any other materials contacting the eyes.

Note: The word *Danger* is used in this manual to indicate procedures that require extra precautions to ensure personal safety.

CAUTIONS

Core Storage

Be extremely cautious when working around the core array. Avoid disturbing individual planes. Sense and select wires are welded to pins at the perimeter of the array.

Bending these pins can fracture welds or cause shorts between adjacent pins. Use the handles provided and exercise care to prevent the sides from striking the frame of SLT cards whenever it is necessary to remove the array. Do not leave core storage unit unattended when covers are removed.

Oscilloscope

Core Storage

Direct probing of the core planes is not advised because of the physical construction of the core array. Techniques for obtaining current and voltage wave shapes are detailed in section 1.7.6 of this manual.

General

The SLT probe tip should be used when scoping to prevent shorting of voltage pins. Probing with alligator clips or uninsulated tips should be avoided.

Power Supplies

When the system is in a power-off status, 24 vac is present in the power supply area, and 110 vac power is present at the convenience outlets.

SLT Components

Turn off power whenever an SLT card is removed or replaced. Turn off power to the system when wrapping or unwrapping wire or when testing for continuity.

Avoid operating the system for prolonged periods of time with the SLT card covers removed.

Servicing

Clear core storage after servicing the processor to prevent returning the system to the customer with an invalid word in core storage. An invalid word results in a parity error when the word is read from core.

Tying input and output logic functions to ground or to 0 volt level can be helpful in troubleshooting. Exercise care in the disk storage unit to prevent destroying disk storage data when tying lines to the 0 volt level. Some logic blocks can be tied to the +3 volt level. It is necessary to evaluate the physical construction of the component circuits, both input and output, on a line before it can be determined whether the +3 volt level will be effective. Information about the component circuits is not now available in the field. In general, use a 0 volt level and work back to an input or an output which gives the required +3 volt level.

Power supply voltages are present on some pins. Exercise care not to ground these pins.

Note: Insert a 470 ohm resistor to act as a load-limiting resistor in the jumper used for tying down lines.

Card Read Punch I/O

Run all cards out of the card read punch before powering down. Powering down the card read punch when the card punch is loaded with cards may result in a card laced in column 1. Use the provided diagnostic tests as masters and reproduce the deck before using it. This procedure will reduce re-keypunching of cards. Make the customer aware of the lacing of cards.

Note: The word *Caution* is used in this manual to indicate procedures that require extra precautions to prevent machine damage.

Rapid and effective trouble diagnosis depends upon a thorough knowledge of the machine logic and data flow, as well as the effective use of diagnostic aids and maintenance features. This chapter presents reference data and service aids to guide the error analysis activity in a logical and straightforward manner.

There are five basic models of the 1131 (models 1 through 5). Figure 1-1 shows the differences between the models and the variations within all the model groupings. Figure 1-2 shows all basic and optional features for the 1131.

1131 CPU Model	Core-Storage Cycle Time*	Core-Storage Capacity (in 16-bit words)	Internal Disk Storage	Input Power (U.S.A. only)
1A	3.6	4k	No	115 vac
1B	3.6	8k	No	115 vac
1C	3.6	16k	No	208/230 vac
1D	3.6	32k	No	208/230 vac
2A	3.6	4k	Yes	115 vac
2B	3.6	8k	Yes	115 vac
2C	3.6	16k	Yes	208/230 vac
2D	3.6	32k	Yes	208/230 vac
3B	2.2	8k	Yes	208/230 vac
3C	2.2	16k	Yes	208/230 vac
3D	2.2	32k	Yes	208/230 vac
4A	3.6	4k	Yes	115 vac
4B	3.6	8k	Yes	115 vac
5B	2.2	8k	No	208/230 vac
5C	2.2	16k	No	208/230 vac
5D	2.2	32k	No	208/230 vac

*Core storage time is in microseconds. For Models 1, 2, 3, and 5 machine cycle time is the same as storage cycle time. For the Model 4, the machine cycle time is 5.85 microseconds. Machine cycle time is the time required for the CPU to perform one step in the execution of an instruction.

Figure 1-1. 1131 Model Variations

This page intentionally blank.

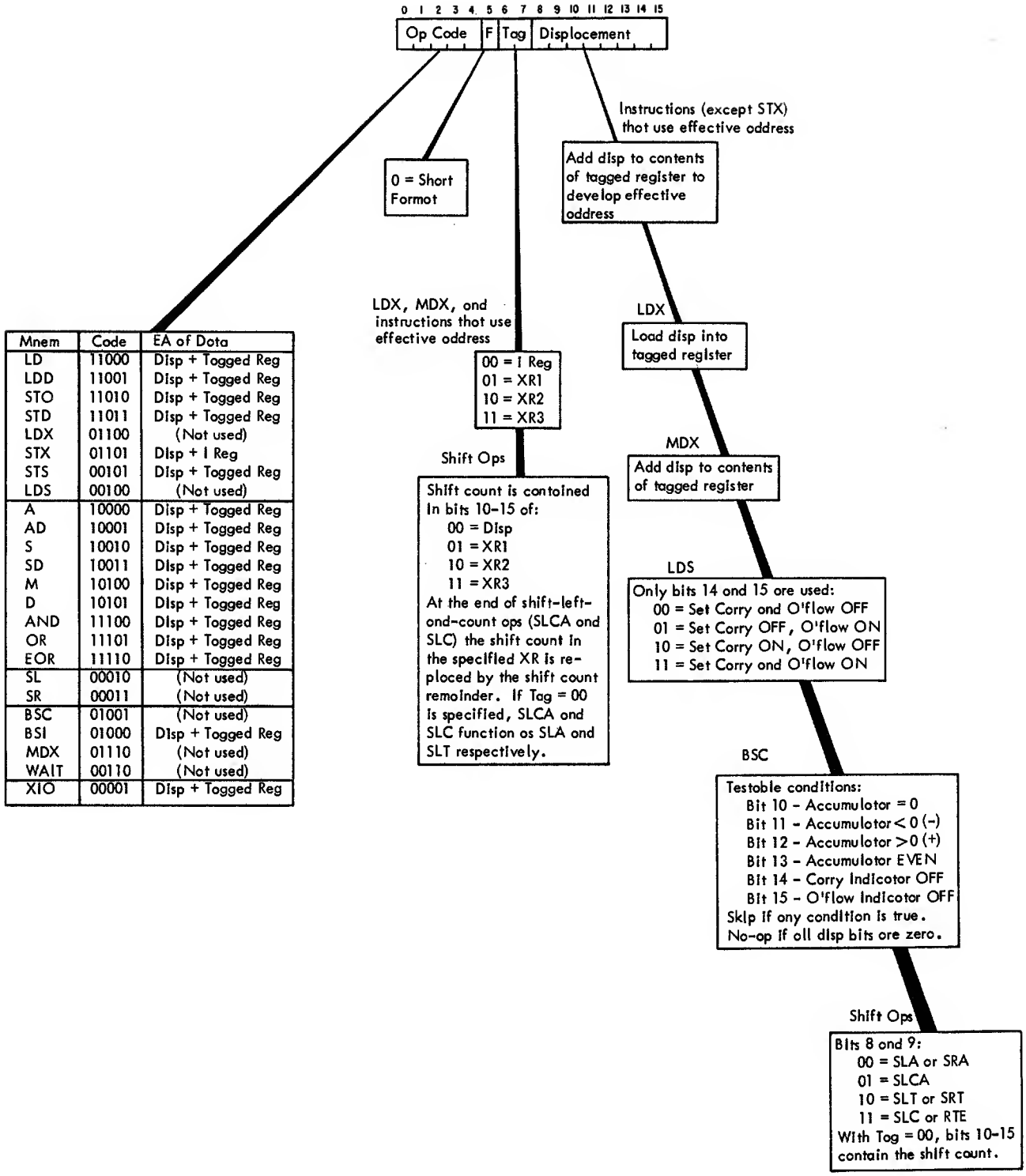
Basic Features	1131 Model				
	1*	2*	3	4‡‡	5
Cansole Keybaard	A, B, C, and D	A, B, C, and D	B, C, and D	A and B	B, C, and D
Cansole Printer	A, B, C, and D	A, B, C, and D	B, C, and D	A and B	B, C, and D
3.6 µs Care Starage	A, B, C, and D	A, B, C, and D		A and B	
115 vac Pawer	A and B	A and B		A and B	
Single Disk Starage		A, B, C, and D	B, C, and D	A and B	
2.2 µs Care Starage			B, C, and D		B, C, and D
208 vac Pawer (60 Hz)	C and D	C and D	B, C, and D		B, C, and D
Optianal Features					
208 vac Power (60 Hz)	A and B	A and B		A and B	
1055 Paper Tape Punch	A, B, C, and D	A, B, C, and D	B, C, and D		B, C, and D
1132 Printer Model 1	A, B, C, and D	A, B, C, and D	B, C, and D		B, C, and D
1132 Printer Madel 2				A and B	
1134 Paper Tape Reader	A, B, C, and D	A, B, C, and D	B, C, and D		B, C, and D
1442 Models 6 and 7 Card Read Punch	A, B, C, and D	A, B, C, and D	B, C, and D	A and B****	B, C, and D
1627 Plotter	A, B, C, and D	A, B, C, and D	B, C, and D	A and B	B, C, and D
Synchronous Communications Adapter	A, B, C, and D	A, B, C, and D	B, C, and D		B, C, and D
Storage Access Channel I (SAC)	A, B, C, and D	A, B, C, and D	B, C, and D		B, C, and D
1133 Multiplexer Control	B, C, and D	A and B‡, C and D†	B, C, and D†		B, C, and D
2310 B Disk Storage		A, B, C, and D**	B, C, and D**		B, C, and D**
2311 Disk Starage	B, C, and D**	A, B, C, and D**	B, C, and D**		B, C, and D**
1403 Printer	B, C, and D**	A, B, C, and D**	B, C, and D**		B, C, and D**
Starage Access Channel II (SAC II)¤	B, C, and D**	A, B, C, and D**	B, C, and D**		B, C, and D**
2501 Card Reader ***	B, C, and D†††	A and B‡, C and D	B, C, and D		B, C, and D
1442 Madel 5 Card Punch	A, B, C, and D	A and B‡, C and D	B, C, and D		B, C, and D
1231 Optical Mark Page Reader ***	B, C, and D†††	A and B‡, C and D	B, C, and D		B, C, and D
2250 Madel 4 Display Unit ††	B, C, and D	B, C, and D	B, C, and D		B, C, and D
IBM System/7	B, C, and D	B, C, and D	B, C, and D		B, C, and D

* Model 1 can be field changed ta Madel 2 ar 3.
Model 2 can be field changed ta Madel 3.
(Only systems with midpock power supplies can be upgraded, in the field, to a Model 3D.)
† Storage Access Channel 1 required an all madels.
†† Storage Access Channel and Card Reader required.
††† Disk Starage required.
‡ 208 vac ar 230 vac 60 Hz power feature required in U.S.A. an Madels A and B.
** 1133 Multiplexer Cantrol required on all models.
¤ Required ta cannect any device or devices previously connected ta SAC when an 1133 Multiplexer Cantrol is connected ta SAC.
*** A system can nat have both a 2501 and a 1231.
**** 1442 Madel 6 ar 7 is basic an 1131 Model 4.
‡‡ 1131 Madel 4 cycle time is 5.85 µs.

Figure 1-2. Basic and Optional Features for the 1130 System

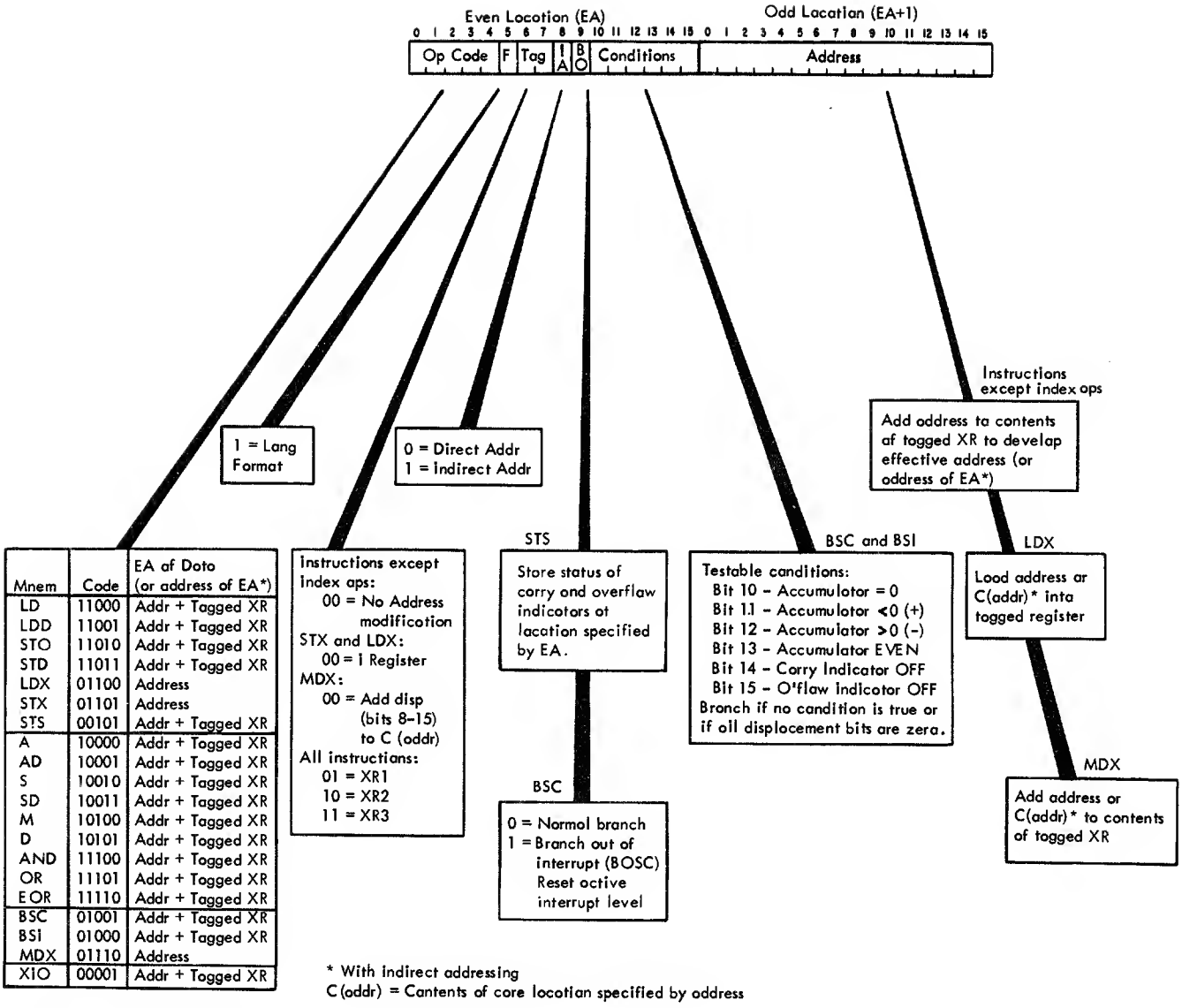
Section 1. Reference Data

Figures 1-3 through 1-31 contain reference data for use in servicing the IBM 1130 Computing System.



Mnem	Code	EA of Data
LD	11000	Disp + Tagged Reg
LDD	11001	Disp + Tagged Reg
STO	11010	Disp + Tagged Reg
STD	11011	Disp + Tagged Reg
LDX	01100	(Not used)
STX	01101	Disp + I Reg
STS	00101	Disp + Tagged Reg
LDS	00100	(Not used)
A	10000	Disp + Tagged Reg
AD	10001	Disp + Tagged Reg
S	10010	Disp + Tagged Reg
SD	10011	Disp + Tagged Reg
M	10100	Disp + Tagged Reg
D	10101	Disp + Tagged Reg
AND	11100	Disp + Tagged Reg
OR	11101	Disp + Tagged Reg
EOR	11110	Disp + Tagged Reg
SL	00010	(Not used)
SR	00011	(Not used)
BSC	01001	(Not used)
BSI	01000	Disp + Tagged Reg
MDX	01110	(Not used)
WAIT	00110	(Not used)
XIO	00001	Disp + Tagged Reg

Figure 1-3. Short Instruction Format



Mnem	Code	EA of Data (or address of EA*)
LD	11000	Addr + Tagged XR
LDD	11001	Addr + Tagged XR
STO	11010	Addr + Tagged XR
STD	11011	Addr + Tagged XR
LDX	01100	Address
STX	01101	Address
STS	00101	Addr + Tagged XR
A	10000	Addr + Tagged XR
AD	10001	Addr + Tagged XR
S	10010	Addr + Tagged XR
SD	10011	Addr + Tagged XR
M	10100	Addr + Tagged XR
D	10101	Addr + Tagged XR
AND	11100	Addr + Tagged XR
OR	11101	Addr + Tagged XR
EOR	11110	Addr + Tagged XR
BSC	01001	Addr + Tagged XR
BSI	01000	Addr + Tagged XR
MDX	01110	Address
XIO	00001	Addr + Tagged XR

Figure 1-4. Long Instruction Format

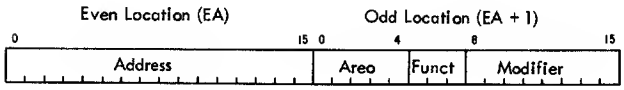


Figure 1-5. IOCC Format

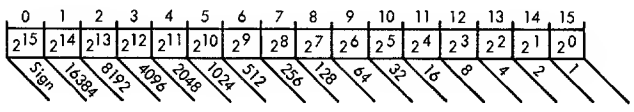


Figure 1-6. Single-Precision Data Word

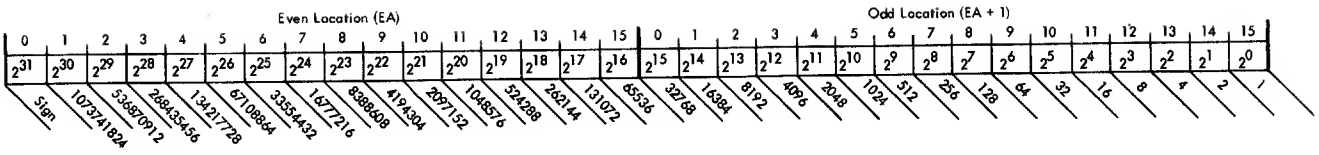


Figure 1-7. Double-Precision Data Word

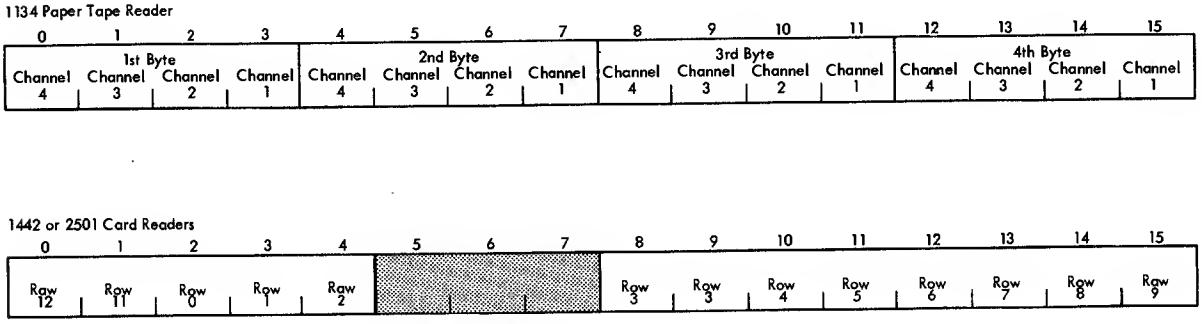


Figure 1-8. Data Words - IPL Mode

Tag	F=0 (Direct Addressing)	F=1, IA=0 (Direct Addressing)	F=1, IA=1 (Indirect Addressing)
T=00	EA=Disp+IAR	EA=Add	EA=C/Add
T=01	EA=Disp+XR1	EA=Add+XR1	EA=C/(Add+XR1)
T=10	EA=Disp+XR2	EA=Add+XR2	EA=C/(Add+XR2)
T=11	EA=Disp+XR3	EA=Add+XR3	EA=C/(Add+XR3)

Disp=Contents of Displocement field of instruction.

Add=Contents of Address field of instruction.

C=Contents of Locotion specified by Add or Add+XR.

Note: This toble does not opply to the MDX, LDX, STX, LDS, Shift or Woit instructions.

Figure 1-9. Effective Address Computation

Instruction	Mnemonic	Binary OP Code	1131 Models 1 and 2 Execution Times (in microseconds)							
			Single Word (F = 0)				Double Word (F = 1)			
			T = 00		T = 01, 10, or 11		T = 00		T = 01, 10, or 11	
			Avg.	Max.	Avg.	Max.	Avg.[1]	Max.[1]	Avg.[1]	Max.[1]
Load and Store										
Load ACC	LD	11000	7.6	–	11.2	–	10.8	–	14.8	–
Load Double	LDD	11001	11.2	–	14.9	–	14.4	–	18.0	–
Store ACC	STO	11010	7.6	–	11.2	–	10.8	–	14.8	–
Store Double	STD	11011	11.2	–	14.9	–	14.4	–	18.0	–
Load Index	LDX	01100	4.5	–	7.2	–	7.2	–	11.8	–
Store Index	STX	01101	7.6	–	11.2	–	11.8	–	15.4	–
Load Status*	LDS[7]	00100	3.6	–	3.6	–	–	–	–	–
Store Status	STS	00101	7.6	–	11.2	–	10.8	–	14.8	–
Arithmetic										
Add	A	10000	8.0	13.0	11.7	16.6	11.2	16.2	15.3	20.3
Add Double	AD	10001	12.2	22.0	15.8	25.6	15.3	25.2	19.3	29.5
Subtract	S	10010	8.0	13.0	11.7	16.6	11.2	16.2	15.3	20.3
Subtract Double	SD	10011	12.2	22.0	15.8	25.6	15.3	25.2	19.3	29.5
Multiply	M	10100	25.7	40.0	29.3	43.6	29.3	43.6	32.9	47.2
Divide	D	10101	76.0	150.8	79.6	154.4	79.6	154.4	83.2	150.0
AND	AND	11100	7.6	–	11.2	–	10.8	–	14.8	–
OR	OR	11101	7.6	–	11.2	–	10.8	–	14.8	–
Exclusive OR	EOR	11110	7.6	–	11.2	–	10.8	–	14.8	–
Shift Left*,Modifier Bits 8 & 9										
No Operation	NOP	00010	3.6	–	–	–	–	–	–	–
Shift Left ACC,00	SLA[7]	00010								
Shift Left ACC and EXT,10	SLT[7]	00010								
Shift Left and Count ACC,01	SLCA[7,8]	00010								
Shift Left and Count ACC and EXT,11	SLC[7,8]	00010	[3]	–	[4]	–	–	–	–	–
Shift Right*,Modifier Bits 8 & 9										
Shift Right ACC,00 or 01	SRA[7]	00011								
Shift Right ACC and EXT,10	SRT[7]	00011								
Rotate Right,11	RTE[7]	00011	[5]		[6]					
Branch										
Branch and Store IAR	BSI	01000	7.6	–	11.2	–	10.8[2]	–	14.8	–
Branch or Skip on Condition	BSC	01001	3.6	–	3.6	–	7.2[2]	–	11.2	–
Modify Index and Skip	MDX	01110	4.5	9.9	11.2	16.2	18.5	23.4	18.5	23.4
Wait*	WAIT[7]	00110[9]	3.6	–	3.6	–	–	–	–	–
Input/Output										
Execute I/O	XIO[10]	00001	11.2	–	14.8	–	14.4	–	18.4	–

*Valid in short format only

Notes:

1. Indirect addressing, where applicable, adds one storage cycle (3.6 μsec) to execution time.
2. If branch is taken.
3. One storage cycle + 0.45(N-4). When N ≤4, only one storage cycle is used.
4. Two storage cycles + 0.45(N-4). When N≤4, only two storage cycles are used.
5. N > 16: one storage cycle + 0.45(N-19).
   N < 16: one storage cycle + 0.45(N-4).
   When N = 16, only one storage cycle is used.
6. N > 16: two storage cycles + 0.45(N-19).
   N < 16: two storage cycles + 0.45(N-4).
   where N = number of positions shifted,
   When N = 16, only two storage cycles are used.
7. Indirect addressing not allowed.
8. If T = 00, functions as SLA or SLT.
9. All unassigned OP codes are defined as wait operations.
10. If XIO read or write, add one storage cycle.

Figure 1-10 (Part 1 of 3). Instruction Codes and Execution Times

Instruction	Mnemonic	Binary OP Code	1131 Models 3 and 5 Execution Times (in microseconds)							
			Single Word (F = 0)				Double Word (F = 1)			
			T = 00		T = 01, 10, or 11		T = 00		T = 01, 10, or 11	
			Avg.	Max.	Avg.	Max.	Avg.[1]	Max.[1]	Avg.[1]	Max.[1]
Load and Store										
Load ACC	LD	11000	4.6	–	6.8	–	6.6	–	9.0	–
Load Double	LDD	11001	6.8	–	9.1	–	8.8	–	11.0	–
Store ACC	STO	11010	4.6	–	6.8	–	6.6	–	9.0	–
Store Double	STD	11011	6.8	–	9.1	–	8.8	–	11.0	–
Load Index	LDX	01100	2.7	–	4.4	–	4.4	–	7.2	–
Store Index	STX	01101	4.6	–	6.8	–	7.2	–	9.4	–
Load Status*	LDS[7]	00100	2.2	–	2.2	–	–	–	–	–
Store Status	STS	00101	4.6	–	6.8	–	6.6	–	9.0	–
Arithmetic										
Add	A	10000	4.9	7.9	7.1	10.1	6.8	9.9	9.4	12.4
Add Double	AD	10001	7.5	13.4	9.6	15.6	9.4	15.4	11.8	18.0
Subtract	S	10010	4.9	7.9	7.1	10.1	6.8	9.9	9.4	12.4
Subtract Double	SD	10011	7.5	13.4	9.6	15.6	9.4	15.4	20.1	26.1
Multiply	M	10100	15.7	24.4	17.9	26.6	17.9	26.6	18.8	28.8
Divide	D	10101	46.4	92.1	48.6	94.4	48.6	94.4	50.8	91.6
AND	AND	11100	4.6	–	6.8	–	6.6	–	9.0	–
OR	OR	11101	4.6	–	6.8	–	6.6	–	9.0	–
Exclusive OR	EOR	11110	4.6	–	6.8	–	6.6	–	9.0	–
Shift Left*,Modifier 8its 8 & 9										
No Operation	NOP	00010	2.2	–	–	–	–	–	–	–
Shift Left ACC,00	SLA[7]	00010								
Shift Left ACC and EXT,10	SLT[7]	00010								
Shift Left and Count ACC,01	SLCA[7] [8]	00010								
Shift Left and Count ACC and EXT,11	SLC[7] [8]	00010	[3]	–	[4]	–	–	–	–	–
Shift Right*,Modifier 8its 8 & 9										
Shift Right ACC,00 or 01	SRA[7]	00011								
Shift Right ACC and EXT,10	SRT[7]	00011								
Rotate Right,11	RTE[7]	00011	[5]		[6]					
Branch										
Branch and Store IAR	BSI	01000	4.6	–	6.8	–	6.6[2]	–	9.0	–
Branch or Skip on Condition	BSC	01001	2.2	–	2.2	–	4.4[2]	–	6.8	–
Modify Index and Skip	MDX	01110	2.7	6.0	6.8	9.9	11.3	14.3	11.3	14.3
Wait*	WAIT[7]	00110[9]	2.2	–	2.2	–	–	–	–	–
Input/Output										
Execute I/O	XIO[10]	00001	6.8	–	9.0	–	8.8	–	11.2	–

*Valid in short format only

Notes:

1. Indirect addressing, where applicable, adds one storage cycle (2.2 μsec) to execution time.
2. If branch is taken.
3. One storage cycle + 0.275(N-4). When N ≤4, only one storage cycle is used.
4. Two storage cycles + 0.275(N-4). When N ≤4, only two storage cycles are used.
5. N > 16: one storage cycle + 0.275(N-19).
   N < 16: one storage cycle + 0.275(N-4).
   When N = 16, only one storage cycle is used.
6. N > 16: two storage cycles + 0.275(N-19).
   N < 16: two storage cycles + 0.275(N-4),
   where N = number of positions shifted.
   When N = 16, only two storage cycles are used.
7. Indirect addressing not allowed.
8. If T = 00, functions as SLA or SLT.
9. All unassigned OP codes are defined as wait operations.
10. If XIO read or write, add one storage cycle.

Figure 1-10 (Part 2 of 3). Instruction Codes and Execution Times

Instruction	Mnemonic	Binary Op Code	1131 Model 4 Execution Times (in microseconds)**							
			Single Word (F = 0)				Double Word (F = 1)			
			T = 00		T = 01, 10 or 11		T = 00		T = 01, 10, or 11	
			Avg.	Max.	Avg.	Max.	Avg.[1]	Max.[1]	Avg.[1]	Max.[1]
Load and Store										
Load ACC	LD	11000	12.1	–	18.0	–	17.5	–	23.8	–
Load Double	LDD	11001	18.0	–	23.8	–	23.4	–	29.2	–
Store ACC	STO	11010	12.1	–	18.0	–	17.5	–	23.8	–
Store Double	STD	11011	18.0	–	23.8	–	23.4	–	29.2	–
Load Index	LDX	01100	6.8	–	11.7	–	11.7	–	18.5	–
Store Index	STX	01101	12.1	–	18.0	–	18.5	–	24.3	–
Load Status*	LDS[7]	00100	5.9	–	5.9	–	–	–	–	–
Store Status	STS	00101	12.1	–	18.0	–	17.5	–	23.8	–
Arithmetic										
Add	A	10000	12.6	19.8	18.4	25.6	18.0	25.2	24.3	31.5
Add Double	AD	10001	18.9	35.5	24.8	41.5	24.3	40.9	30.6	47.7
Subtract	S	10010	12.6	19.8	18.4	25.6	18.0	25.2	24.3	31.5
Subtract Double	SD	10011	18.9	35.5	24.8	41.5	24.3	40.9	30.6	47.7
Multiply	M	10100	41.4	64.8	47.5	70.6	47.5	70.6	53.1	76.5
Divide	D	10101	123.3	243.0	129.1	248.8	129.1	248.8	135.0	242.1
AND	AND	11100	12.1	–	18.0	–	17.5	–	23.8	–
OR	OR	11101	12.1	–	18.0	–	17.5	–	23.8	–
Exclusive OR	EOR	11110	12.1	–	18.0	–	17.5	–	23.8	–
Shift Left*,Modifier Bits 8 & 9										
No Operation	NOP	00010	5.9	–	–	–	–	–	–	–
Shift Left ACC,00	SLA[7]	00010								
Shift Left ACC and EXT,10	SLT[7]	00010								
Shift Left and Count ACC,01	SLCA[7] [8]	00010								
Shift Left and Count ACC and EXT,11	SLC[7] [8]	00010	[3]	–	[4]	–	–	–	–	–
Shift Right*,Modifier Bits 8 & 9										
Shift Right ACC,00 or 01	SRA[7]	00011								
Shift Right ACC and EXT,10	SRT[7]	00011								
Rotate Right,11	RTE[7]	00011	[5]		[6]					
Branch										
Branch and Store IAR	BSI	01000	12.1	–	18.0	–	17.5[2]	–	23.8	–
Branch or Skip on Condition	BSC	01001	5.9	–	5.9	–	11.7[2]	–	18.0	–
Modify Index and Skip	MDX	01110	6.8	14.4	18.0	25.2	29.6	36.9	29.6	36.9
Wait*	WAIT[7]	00110[9]	5.9	–	5.9	–	–	–	–	–
Input/Output										
Execute I/O	XIO[10]	00001	18.0	–	23.8	–	23.4	–	29.5	–

*Valid in short format only

**Execution times are the same as for Models 1 and 2 when either interruption level 0 or 1 is active.

Notes:

1. Indirect addressing, where applicable, adds one storage cycle (5.9 or 3.6 μsec) to execution time.
2. If branch is taken.
3. One storage cycle + 0.45(N-4). When ≤4, only one storage cycle is used.
4. Two storage cycles + 0.45(N-4). When ≤4, only two storage cycles are used.
5. N > 16: one storage cycle + 0.45(N-19).
   N < 16: one storage cycle + 0.45(N-4).
   When N = 16, only one storage cycle is used.
6. N > 16: two storage cycles + 0.45(N-19).
   N < 16: two storage cycles + 0.45(N-4),
   where N = number of positions shifted.
   When N = 16, only two storage cycles are used.
7. Indirect addressing not allowed.
8. If T = 00, functions as SLA or SLT.
9. All unassigned OP codes are defined as wait operations.
10. If XIO read or write, add one storage cycle.

Figure 1-10 (Part 3 of 3). Instruction Codes and Execution Times

Instruction	Tag Bits	Register/Operation
Load Index	00	IAR
Store Index	01	XR1
	10	XR2
	11	XR3
Shift Left	00	Disp
Shift Right	01	XR1
	10	XR2
	11	XR3
Modify Index and Skip		
F = 0	00	Disp added to IAR
	01	Disp added to XR1
	10	Disp added to XR2
	11	Disp added to XR3
F = 1; IA = 0	00	+ Disp added to C
	01	Add added to XR1
	10	Add added to XR2
	11	Add added to XR3
F = 1; IA = 1	00	-Disp added to C
	01	C added to XR1
	10	C added to XR2
	11	C added to XR3

Disp = Contents of displacement field of instruction

Add = Contents of address field of instruction

C = Contents of location specified by add

Figure 1-11. Tag Bit Codes

Bit Position	Condition
10	ACC zero
11	ACC negative
12	ACC positive, not zero
13	ACC even
14	Carry Indicatar OFF
15	Overflow Indicator OFF

Short Instruction
Skip if any one condition is true.
No-Op if all bits are zero.

Long Instruction
Branch if none of the conditions are true.
Unconditional branch if all bits are zero.

Figure 1-12. BSC Condition Codes

B Reg (Core) → Acc →	Results in Acc		
	AND	OR	EOR
0 → 0 →	0	0	0
0 → 1 →	0	1	1
1 → 0 →	0	1	1
1 → 1 →	1	1	0

Figure 1-13. AND, OR, EOR Operations

Hexadecimal	Load and Store Instructions
	Load Accumulator (LD)
C0XX	Contents of CSL at EA (I+DISP) are loaded into A
C1XX	Contents of CSL at EA (XR1+DISP) are loaded into A
C2XX	Contents of CSL at EA (XR2+DISP) are loaded into A
C3XX	Contents of CSL at EA (XR3+DISP) are loaded into A
C400XXXX	Contents of CSL at EA (Addr) are loaded into A
C500XXXX	Contents of CSL at EA (Addr +XR1) are loaded into A
C600XXXX	Contents of CSL at EA (Addr +XR2) are loaded into A
C700XXXX	Contents of CSL at EA (Addr +XR3) are loaded into A
C480XXXX	Contents of CSL at EA (V in CSL at Addr) are loaded into A
C580XXXX	Contents of CSL at EA (V in CSL at "Addr +XR1") are loaded into A
C680XXXX	Contents of CSL at EA (V in CSL at "Addr +XR2") are loaded into A
C780XXXX	Contents of CSL at EA (V in CSL at "Addr +XR3") are loaded into A
	Double Load (LDD)
C8XX	Contents of CSL at EA (I + DISP) and EA+1 are loaded into A and Q
C9XX	Contents of CSL at EA(XR1 + DISP) and EA+1 are loaded into A and Q
CAXX	Contents of CSL at EA (XR2 + DISP) and EA+1 are loaded into A and Q
CBXX	Contents of CSL at EA (XR3 + DISP) and EA+1 are loaded into A and Q
CC00XXXX	Contents of CSL at EA (Addr) and EA+1 are loaded into A and Q
CD00XXXX	Contents of CSL at EA (Addr +XR1) and EA+1 are loaded into A and Q
CE00XXXX	Contents of CSL at EA (Addr +XR2) and EA+1 are loaded into A and Q
CF00XXXX	Contents of CSL at EA (Addr +XR3) and EA+1 are loaded into A and Q
CC80XXXX	Contents of CSL at EA (V in CSL at Addr) and EA+1 are loaded into A and Q
CD80XXXX	Contents of CSL at EA (V in CSL at "Addr +XR1") and EA+1 are loaded into A and Q
CE80XXXX	Contents of CSL at EA (V in CSL at "ADDR +XR2") and EA+1 are loaded into A and Q
CF80XXXX	Contents of CSL at EA (V in CSL at "Addr +XR3") and EA+1 are loaded into A and Q
	Store Accumulator (STO)
D0XX	Contents of A are stored in CSL at EA (I+DISP)
D1XX	Contents of A are stored in CSL at EA (XR1+DISP)
D2XX	Contents of A are stored in CSL at EA (XR2+DISP)
D3XX	Contents of A are stored in CSL at EA (XR3+DISP)
D400XXXX	Contents of A are stored in CSL at EA (Addr)
D500XXXX	Contents of A are stored in CSL at EA (Addr +XR1)
D600XXXX	Contents of A are stored in CSL at EA (Addr +XR2)
D700XXXX	Contents of A are stored in CSL at EA (Addr +XR3)
D480XXXX	Contents of A are stored in CSL at EA (V in CSL at Addr)
D580XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr +XR1")
D680XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr +XR2")
D780XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr +XR3")
	Double Store (STD)
D8XX	Contents of A and Q are stored in CSL at EA (I+DISP) and EA+1
D9XX	Contents of A and Q are stored in CSL at EA (XR1 +DISP) and EA+1
DAXX	Contents of A and Q are stored in CSL at EA (XR2 +DISP) and EA+1
DBXX	Contents of A and Q are stored in CSL at EA (XR3 +DISP) and EA+1
DC00XXXX	Contents of A and Q are stored in CSL at EA (Addr) and EA+1
DD00XXXX	Contents of A and Q are stored in CSL at EA (Addr +XR1) and EA+1
DE00XXXX	Contents of A and Q are stored in CSL at EA (Addr +XR2) and EA+1
DF00XXXX	Contents of A and Q are stored in CSL at EA (Addr +XR3) and EA+1
DC80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at Addr) and EA+1
DD80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR1") and EA+1
DE80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR2") and EA+1
DF80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR3") and EA+1
	Load Index (LDX)
60XX	Load DISP into the Instruction Register
61XX	Load DISP into Index Register 1
62XX	Load DISP into Index Register 2
63XX	Load DISP into Index Register 3
6400XXXX	Load Addr into the Instruction Register
6500XXXX	Load Addr into Index Register 1
6600XXXX	Load Addr into Index Register 2

Hexadecimal	Load and Store Instructions
	Load Index (LDX)
6700XXXX	Load Addr into Index Register 3
6480XXXX	Load contents of CSL at Addr into the Instruction Register
6580XXXX	Load contents of CSL at Addr into Index Register 1
6680XXXX	Load contents of CSL at Addr into Index Register 2
6780XXXX	Load contents of CSL at Addr into Index Register 3
	Store Index (STX)
68XX	Store I in CSL at EA (I+DISP)
69XX	Store XR1 in CSL at EA (I+DISP)
6AXX	Store XR2 in CSL at EA (I+DISP)
6BXX	Store XR3 in CSL at EA (I+DISP)
6C00XXXX	Store I in CSL at EA (Addr)
6D00XXXX	Store XR1 in CSL at EA (Addr)
6E00XXXX	Store XR2 in CSL at EA (Addr)
6F00XXXX	Store XR3 in CSL at EA (Addr)
6C80XXXX	Store I in CSL at EA (V in CSL at Addr)
6D80XXXX	Store XR1 in CSL at EA (V in CSL at Addr)
6E80XXXX	Store XR2 in CSL at EA (V in CSL at Addr)
6F80XXXX	Store XR3 in CSL at EA (V in CSL at Addr)
	Store Status (STS)
28XX	Store status of indicators in CSL at EA (I+DISP)
29XX	Store status of indicators in CSL at EA (XR1+DISP)
2AXX	Store status of indicators in CSL at EA (XR2+DISP)
2BXX	Store status of indicators in CSL at EA (XR3+DISP)
2C00XXXX	Store status of indicators in CSL at EA (Addr)
2D00XXXX	Store status of indicators in CSL at EA (Addr+XR1)
2E00XXXX	Store status of indicators in CSL at EA (Addr+XR2)
2F00XXXX	Store status of indicators in CSL at EA (Addr+XR3)
2C80XXXX	Store status of indicators in CSL at EA (V in CSL at Addr)
2D80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr +XR1")
2E80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr +XR2")
2F80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr +XR3")
	Load Status (LDS)
2000	Set CARRY and OVERFLOW indicators OFF
2001	Set OVERFLOW ON and CARRY OFF
2002	Set OVERFLOW OFF and CARRY ON
2003	Set CARRY and OVERFLOW indicator ON
	Arithmetic Instructions
	Add (A)
80XX	Add contents of CSL at EA (I+DISP) to A
81XX	Add contents of CSL at EA (XR1+DISP) to A
82XX	Add contents of CSL at EA (XR2+DISP) to A
83XX	Add contents of CSL at EA (XR3+DISP) to A
8400XXXX	Add contents of CSL at EA (Addr) to A
8500XXXX	Add contents of CSL at EA (Addr +XR1) to A
8600XXXX	Add contents of CSL at EA (Addr +XR2) to A
8700XXXX	Add contents of CSL at EA (Addr +XR3) to A
8480XXXX	Add contents of CSL at EA (V in CSL at Addr) to A
8580XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR1") to A
8680XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR2") to A
8780XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR3") to A
	Double Add (AD)
88XX	Add contents of CSL at EA (I+DISP) and EA+1 to A and Q
89XX	Add contents of CSL at EA (XR1+DISP) and EA+1 to A and Q
8AXX	Add contents of CSL at EA (XR2+DISP) and EA+1 to A and Q
8BXX	Add contents of CSL at EA (XR3+DISP) and EA+1 to A and Q
8C00XXXX	Add contents of CSL at EA (Addr) and EA+1 to A and Q
8D00XXXX	Add contents of CSL at EA (Addr+XR1) and EA+1 to A and Q
8E00XXXX	Add contents of CSL at EA (Addr+XR2) and EA+1 to A and Q
8F00XXXX	Add contents of CSL at EA (Addr+XR3) and EA+1 to A and Q
8C80XXXX	Add contents of CSL at EA (V in CSL at Addr) and EA+1 to A and Q
8D80XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1 to A and Q
8E80XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1 to A and Q

Figure 1-14. Instruction Set (Part 1)

Hexadecimal	Arithmetic Instructions
8F80XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1 to A and Q
	Subtract (S)
90XX	Subtract contents of CSL at EA (I+DISP) from A
91XX	Subtract contents of CSL at EA (XR1+DISP) from A
92XX	Subtract contents of CSL at EA (XR2+DISP) from A
93XX	Subtract contents of CSL at EA (XR3+DISP) from A
9400XXXX	Subtract contents of CSL at EA (Addr) from A
9500XXXX	Subtract contents of CSL at EA (Addr+XR1) from A
9600XXXX	Subtract contents of CSL at EA (Addr+XR2) from A
9700XXXX	Subtract contents of CSL at EA (Addr+XR3) from A
9480XXXX	Subtract contents of CSL at EA (V in CSL at Addr) from A
9580XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR1") from A
9680XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR2") from A
9780XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR3") from A
	Double Subtract (SD)
98XX	Subtract contents of CSL at EA (I+DISP) and EA+1 from A and Q
99XX	Subtract contents of CSL at EA (XR1+DISP) and EA+1 from A and Q
9AXX	Subtract contents of CSL at EA (XR2+DISP) and EA+1 from A and Q
9BXX	Subtract contents of CSL at EA (XR3+DISP) and EA+1 from A and Q
9C00XXXX	Subtract contents of CSL at EA (Addr) and EA+1 from A and Q
9D00XXXX	Subtract contents of CSL at EA (Addr+XR1) and EA+1 from A and Q
9E00XXXX	Subtract contents of CSL at EA (Addr+XR2) and EA+1 from A and Q
9F00XXXX	Subtract contents of CSL at EA (Addr+XR3) and EA+1 form A and Q
9C80XXXX	Subtract contents of CSL at EA (V in CSL at Addr) and EA+1 from A and Q
9D80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1 from A and Q
9E80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1 from A and Q
9F80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1 from A and Q
	Multiply M
A0XX	Multiply contents of CSL at EA (I+DISP) by A
A1XX	Multiply contents of CSL at EA (XR1+DISP) by A
A2XX	Multiply contents of CSL at EA (XR2+DISP) by A
A3XX	Multiply contents of CSL at EA (XR3+DISP) by A
A400XXXX	Multiply contents of CSL at EA (Addr) by A
A500XXXX	Multiply contents of CSL at EA (Addr+XR1) by A
A600XXXX	Multiply contents of CSL at EA (Addr+XR2) by A
A700XXXX	Multiply contents of CSL at EA (Addr+XR3) by A
A480XXXX	Multiply contents of CSL at EA (V in CSL at Addr) by A
A580XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR1") by A
A680XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR2") by A
A780XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR3") by A
	Divide (D)
A8XX	Divide A and O by contents of CSL at EA (I+DISP)
A9XX	Divide A and Q by contents of CSL at EA (XR1+DISP)
AAXX	Divide A and Q by contents of CSL at EA (XR2+DISP)
ABXX	Divide A and Q by contents of CSL at EA (XR3+DISP)
AC00XXXX	Divide A and Q by contents of CSL at EA (Addr)
AD00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR1)
AE00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR2)
AF00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR3)
AC80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at Addr)
AD80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR1")
AE80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR2")
AF80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR3")
	Logical And (AND)
E0XX	AND contents of CSL at EA (I+DISP) with A
E1XX	AND contents of CSL at EA (XR1+DISP) with A
E2XX	AND contents of CSL at EA (XR2+DISP) with A
E3XX	AND contents of CSL at EA (XR3+DISP) with A
E400XXXX	AND contents of CSL at EA (Addr) with A
E500XXXX	AND contents of CSL at EA (Addr+XR1) with A
E600XXXX	AND contents of CSL at EA (Addr+XR2) with A
E700XXXX	AND contents of CSL at EA (Addr+XR3) with A
E480XXXX	AND contents of CSL at EA (V in CSL at Addr) with A
E580XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR1") with A
E680XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR2") with A
E780XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR3") with A

Hexadecimal	Arithmetic Instructions
	Logical Or (OR)
E8XX	OR contents of CSL at EA (I+DISP) with A
E9XX	OR contents of CSL at EA (XR1+DISP) with A
EAXX	OR contents of CSL at EA (XR2+DISP) with A
EBXX	OR contents of CSL at EA (XR3+DISP) with A
EC00XXXX	OR contents of CSL at EA (Addr) with A
ED00XXXX	OR contents of CSL at EA (Addr+XR1) with A
EE00XXXX	OR contents of CSL at EA (Addr+XR2) with A
EF00XXXX	OR contents of CSL at EA (Addr+XR3) with A
EC80XXXX	OR contents of CSL at EA (V in CSL at Addr) with A
ED80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR1") with A
EE80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR2") with A
EF80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR3") with A
	Logical Exclusive Or (EOR)
F0XX	EOR contents of CSL at EA (I+DISP) with A
F1XX	EOR contents of CSL at EA (XR1+DISP) with A
F2XX	EOR contents of CSL at EA (XR2+DISP) with A
F3XX	EOR contents of CSL at EA (XR3+DISP) with A
F400XXXX	EOR contents of CSL at EA (Addr) with A
F500XXXX	EOR contents of CSL at EA (Addr+XR1) with A
F600XXXX	EOR contents of CSL at EA (Addr+XR2) with A
F700XXXX	EOR contents of CSL at EA (Addr+XR3) with A
F480XXXX	EOR contents of CSL at EA (V in CSL at Addr) with A
F580XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR1") with A
F680XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR2") with A
F780XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR3") with A
	Shift Instructions
	Shift Left Logical A (SLA)
10*X	Contents of A shift left the number of shift counts in DISP
1100	Contents of A shift left the number of shift counts in XR1
1200	Contents of A shift left the number of shift counts in XR2
1300	Contents of A shift left the number of shift counts in XR3
	Shift Left Logicol A & O (SLT)
10*X	Contents of A and O shift left the number of shift counts in DISP
1180	Contents of A and O shift left the number of shift counts in XR1
1280	Contents of A and O shift left the number of shift counts in XR2
1380	Contents of A and Q shift left the number of shift counts in XR3
	Shift Left And Count A (SLCA)
10*X	Contents of A shift left the number of shift counts in DISP
1140	Contents of A shift left the number of shift counts in XR1
1240	Contents of A shift left the number of shift counts in XR2
1340	Contents of A shift left the number of shift counts in XR3
	Shift Left And Count A & O (SLC)
10*X	Contents of A and Q shift left the number of shift counts in DISP
11C0	Contents of A and O shift left the number of shift counts in XR1
12C0	Contents of A and Q shift left the number of shift counts in XR2
13C0	Contents of A and Q shift left the number of shift counts in XR3
	Shift Right Logical A (SRA)
18*X	Contents of A shift right the number of shift counts in DISP
1900	Contents of A shift right the number of shift counts in XR1
1A00	Contents of A shift right the number of shift counts in XR2
1B00	Contents of A shift right the number of shift counts in XR3
	Shift Right A & Q (SRT)
18*X	Contents of A and Q shift right the number of shift counts in DISP
1980	Contents of A and Q shift right the number of shift counts in XR1
1A80	Contents of A and Q shift right the number of shift counts in XR2
1B80	Contents of A and Q shift right the number of shift counts in XR3
	Rotate Right A & Q (RTE)
18*X	Contents of A and Q rotate right the number of counts in DISP
19C0	Contents of A and Q rotate right the number of counts in XR1
1AC0	Contents of A and Q rotate right the number of counts in XR2
1BC0	Contents of A and Q rotate right the number of counts in XR3

Figure 1-14. Instruction Set (Part 2)

Hexadecimal	Branch Instructions
	Branch Or Skip On Condition (BSC or BOSC)
48*X	Skip the next one-word instruction if ANY condition is sensed
4C*XXXXX	Branch to CSL at EA (Addr) on NO condition
4D*XXXXX	Branch to CSL at EA (Addr+XR1) on NO condition
4E*XXXXX	Branch to CSL at EA (Addr+XR2) on NO condition
4F*XXXXX	Branch to CSL at EA (Addr+XR3) on NO condition
4C*XXXXX	Branch to CSL at EA (V in CSL at Addr) on NO condition
4D*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR1") on NO condition
4E*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR2") on NO condition
4F*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR3") on NO condition
	Branch And Store Instruction Register (BSI)
40XX	Store next sequential address in CSL at EA (I+DISP) and Branch to EA+1
41XX	Store next sequential address in CSL at EA (XR1+DISP) and Branch to EA+1
42XX	Store next sequential address in CSL at EA (XR2+DISP) and Branch to EA+1
43XX	Store next sequential address in CSL at EA (XR3+DISP) and Branch to EA+1
44*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr) and Branch to EA+1
45*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR1) and Branch to EA+1
46*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR2) and Branch to EA+1
47*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR3) and Branch to EA+1
44*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at Addr) and Branch to EA+1
45*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR1") and Branch to EA+1
46*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR2") and Branch to EA+1
47*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR3") and Branch to EA+1
	Modify Index and Skip (MDX)
70XX	ADD expanded DISP to I (no skip can occur)
71XX	ADD expanded DISP to XR1
72XX	ADD expanded DISP to XR2
73XX	ADD expanded DISP to XR3
74XXXXXX	Add expanded positive DISP to CSL at Addr (Add to memory)
7500XXXX	Add Addr to XR1
7600XXXX	Add Addr to XR2
7700XXXX	Add Addr to XR3
74XXXXXX	Add expanded negative DISP to CSL at Addr (Add to Memory)
7580XXXX	Add V in CSL at Addr to XR1
7680XXXX	Add V in CSL at Addr to XR2
7780XXXX	Add V in CSL at Addr to XR3

Hexadecimal	Branch Instructions
	Wait (WAIT)
3000	WAIT until manual start or interrupt.
	I/O Instructions
	Execute I/O (XIO)
08XX	Execute IOCC in CSL at EA (I+DISP) and EA+1
09XX	Execute IOCC in CSL at EA (XR1+DISP) and EA+1
0AXX	Execute IOCC in CSL at EA (XR2+DISP) and EA+1
0BXX	Execute IOCC in CSL at EA (XR3+DISP) and EA+1
0C00XXXX	Execute IOCC in CSL at EA (Addr)and EA+1
0D00XXXX	Execute IOCC in CSL at EA (Addr+XR1) and EA+1
0E00XXXX	Execute IOCC in CSL at EA (Addr+XR2) and EA+1
0F00XXXX	Execute IOCC in CSL at EA (Addr+XR3) and EA+1
0C80XXXX	Execute IOCC in CSL at EA (V in CSL at Addr) and EA+1
0D80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR1") and EA+1
0E80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR2") and EA+1
0F80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR3") and EA+1

Symbol	Meaning
A	Accumulator
Q	Accumulator Extension
Addr	Contents of the address portion of a two-word instruction
CSL	Core storage location
DISP	Contents of the displacement portion of a one-word instruction
EA	Effective address (See Figure 1-9)
EA + 1	Next higher address from the effective address
I	Contents of the Instruction Register
V	Value
XR1	Contents of Index Register 1
XR2	Contents of Index Register 2
XR3	Contents of Index Register 3
X	Hexadecimal value can be 0-F
*	Used for hexadecimal values that have limits

Figure 1-14. Instruction Set (Part 3)

I/O Device (Code) Instructions	Function Code	Bit No.	Bit	Modifier Bits Function
Console Printer (00001)				
Write	001			
Sense Device	111	15	1	Reset int. level 4 ind.
Console Keyboard (00001)				
Read	010			
Control (interrupt)	100			
Sense Device	111	15	1	Reset int. level 4 ind.
1442 Card Read Punch (00010)				
Read	010			
Write	001			
Control	100	8	1	Stacker Select
		13	1	Start Read
		14	1	Feed Cycle
		15	1	Start Punch
Sense Device	111	14	1	Reset int. level 4 ind.
		15	1	Reset int. level 0 ind.
1134 Paper Tape Reader (00011)				
1055 Paper Tape Punch (00011)				
Read	010			
Write	001			
Control	100			
Sense Device	111	15	1	Reset int. level 4 ind.
Single Disk Storage (00100)				
2310 Drive 1 or (10001)				
2311 Drive 1, Disk 1				
2310 Drive 2 or (10010)				
2311 Drive 1, Disk 2				
2310 Drive 3 or (10011)				
2311 Drive 1, Disk 3				
2310 Drive 4 or (10100)				
2311 Drive 1, Disk 4				
2311 Drive 1, Disk 5 (10110)				
2311 Drive 2, Disk 1 (10111) 0 0 0 } Modifier bits				
2311 Drive 2, Disk 2 (10111) 0 0 1 } 9, 10, and 11				
2311 Drive 2, Disk 3 (10111) 0 1 0 } required for				
2311 Drive 2, Disk 4 (10111) 0 1 1 } second drive,				
2311 Drive 2, Disk 5 (10111) 1 0 0 } as shown.				
Initiate Write	101	13-15		Sector Address
Initiate Read	110	13-15		Sector Address
		8	0	Read Operation
		8	1	Read-Check Operation
Control	100	13	0	Move access forward
		13	1	Move access backward
	*	2-15		Number of Cylinders
Sense Device	111	15	1	Reset int. level 2 ind.
1627 Plotter (00101)				
Write	001			
Sense Device	111	15	1	Reset int. level 3 ind.
1132 Printer (00110)				
Read Emitter	010			
Control	100	8	1	Start Printer
		9	1	Stop Printer
		13	1	Start Carriage
		14	1	Stop Carriage
		15	1	Space Carriage
Sense Device	111	15	1	Reset int. level 1 ind.
1403 Printer (10101)				
Initiate Write	101			
Control	100			Single Line Space
Write	001*	4	1	Skip to Channel 1
		5	1	Skip to Channel 2
		6	1	Skip to Channel 3
		7	1	Skip to Channel 4
		8	1	Skip to Channel 5
		9	1	Skip to Channel 6
		10	1	Skip to Channel 7
		11	1	Skip to Channel 8
		12	1	Skip to Channel 9
		13	1	Skip to Channel 10
		14	1	Skip to Channel 11
		15	1	Skip to Channel 12
Sense Device	111	15	1	Reset int. level 4 ind.
1231 Optical Mark Page Reader (01000)				
Read	010			Read Operation
Control	100	13	1	Start Read
		14	1	I/O Disconnect
		8	1	Select Stacker
Sense Device	111	15	1	Reset int. level 4 ind.

I/O Device (Code) Instructions	Function Code	Bit No.	Bit	Modifier Bits Function
System/7 1130 Host Attachment (01100)				
Initiate Write	101	15	0	Do not interrupt System/7 for operation end
		15	1	Interrupt System/7 for operation end
		14	0	No EIPL
		14	1	EIPL and temporarily prevent attention and power/thermal interruptions
Initiate Read	110	15	0	Do not interrupt System/7 for operation end
		15	1	Interrupt System/7 for operation end
Control	100	15	0	Transfer word count to attachment
		15	1	Transfer System/7 storage address to attachment
		14	0	No effect; return to basic control status
		14	1	Perform function specified by bit 15 and prevent power/thermal interruptions
		13	0	Permit attention and power/thermal interruptions
		13	1	Prevent attention and power/thermal interruptions
		12	0	Ignore bit 13
		12	1	Perform function specified by bit 13
Sense Device	111	15	0	Do not reset int. level request
		15	1	Reset int. level request
2250 Display Unit (11001)				
Initiate Write	101	8	0	Start Regeneration
		8	1	Set Programmed Function Indicators
Initiate Read	110	11	0	Read 6 status words into core. Reset interrupt req.
		11	1	Read 14 status words into core. Reset interrupt req.
Control	100	8	0	No-operation
		8	1	Reset Display
Sense Device		None		DSW to Acc
		11	1	2250 Addr Reg to Acc
		12	1	2250 Revert Reg to Acc
		13	1	2250 Temp Reg to Acc
		15	1	DSW to Acc Reset interrupt req.
Sense Interrupt (ILSW)--				
All Devices	011			
2501 Card Reader (01001)				
Initiate Read	110			
Sense Device	111	15	1	Reset int. level 4 ind.
Synchronous Communications Adapter (01010)				
Initiate Write	101	9	0	Transmit Condition
		9	1	Adapter Reset
Initiate Read	110	All	0	Receive Condition
		14	1	Turn Off Send/Receive
		15	1	Turn On Send/Receive
Write	001	All	0	Load Buffer From Core
		13	1	Set Sync/Idle Register
		14	1	Turn On Audible Alarm
		15	1	Turn Off Audible Alarm
Read	010	All	0	Load Core From Buffer
		14	1	Diagnostic Read 2
		15	1	Diagnostic Read 1
Control	100	8	1	Enable
		9	1	Disable
		10	1	Start/Stop Timeout
		11	1	Synchronize
		12	1	Diagnostic Mode
		13	1	End Operation
		14	1	Set 6-bit Character Frame
		15	1	Set 7-bit Character Frame
Sense Device	111	15	1	Reset Int. level 1 ind.
Console Entry Switches (00111)				
Read	010			

*Modifier bits located in address word.

Figure 1-15. I/O Function Codes and Modifiers

Device Code		I/O Device	Interrupt (Note 3)		
Binary	Decimal		Level	Core Storage Address	ILSW Bits
00000	0	Not used in the 1130 system			
00001	1	Console Keyboard-Printer	4	00012	1
00010	2	1442 Card Read Punch	0	00008	0
			4	00012	2
00011	3	1134 Paper Tape Reader and 1055 Paper Tape Punch	4	00012	0
00100	4	Single Disk Storage	2	00010	0
00101	5	1627 Plotter	3	00011	0
00110	6	1132 Printer	1	00009	0
00111	7	Console Entry Switches	5	00013	0
01000	8	1231 Optical Mark Page Reader	4	00012	5
01001	9	2501 Card Reader	4	00012	3
01010	10	Synchronous Communication Adapter	1	00009	1
01011	11	Note 1			
01100	12	System/7 1130 Host Attachment	3		4
01101	13	Note 1			
01110	14				
01111	15				
10000	16				
10001	17	2310 Disk Storage, Drive 1 or 2311 Disk Storage, Drive 1, Disk 1	2	00010	1
10010	18	2310 Disk Storage, Drive 2 or 2311 Disk Storage, Drive 1, Disk 2	2	00010	2
10011	19	2310 Disk Storage, Drive 3 or 2311 Disk Storage, Drive 1, Disk 3	2	00010	3
10100	20	2310 Disk Storage, Drive 4 or 2311 Disk Storage, Drive 1, Disk 4	2	00010	4
10101	21	1403 Printer	4	00012	4
10110	22	2311 Disk Storage, Drive 1, Disk 5	2	00010	5
10111	23	2311 Disk Storage, Drive 2, Disks 1 through 5 (Note 2)	2	00010	6-10
11000	24	Note 1			
11001	25	2250 Display Unit	3		4
11010	26	Note 1			
11011	27				
11100	28				
11101	29				
11110	30				
11111	31				

Note 1: Reserved for system expansion. These codes when unused by the 1130 system can be assigned to any of the customer's I/O devices on SAC 1 or SAC 11.

Note 2: Disk selection on the second 2311 is made by modifier bits 9, 10, and 11, and are as follows: Disk 1, 000; Disk 2, 001; Disk 3, 010; Disk 4, 011; Disk 5, 100. Disks 3 and 4 are not used on the 2311 model 12.

Note 3: Level A machines--no ILSW bits on levels 0, 1, 2, 3, and 5.

Figure 1-16. I/O Device Codes and Interrupt Levels

Interrupt Level 0

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1442	Expansion														

Interrupt Level 1

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1132	SCA	Expansion and Customer Use													

Interrupt Level 2

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Disk Storage (1131)	2310 B Drive 1 or 2311 Drive 1 Disk 1	2310 B Drive 2 or 2311 Drive 1 Disk 2	2310 B Drive 3 or 2311 Drive 1 Disk 3	2310 B Drive 4 or 2311 Drive 1 Disk 4	2311 Drive 1 Disk 5	2311 Drive 2 Disk 1	2311 Drive 2 Disk 2	2311 Drive 2 Disk 3	2311 Drive 2 Disk 4	2311 Drive 2 Disk 5	SAC Devices				

Note: Disks 3 and 4 are not used if the 2311 drive is a model 12.

Interrupt Level 3

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1627	Expansion and Customer Use		SAC Device	2250 or System/7	SAC II Devices				Expansion and Customer Use						

Interrupt Level 4

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1134 1055	Console, Keyboard Printer	1442	2501	1403	1231	SAC Devices			Expansion and Customer Use						

Interrupt Level 5

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
*	SAC Devices								Expansion and Customer Use						

*Console Program Stop or Interrupt Run Mode

NOTE: Level A machines -- no ILSW bits on levels 0, 1, 2, 3, and 5.

Figure 1-17. 1131 Interrupt Level Status Word (ILSW) Assignments

Figure 1-18. (Deleted, see Figure 1-16)

	**1130-A and C	*1130-B
CS Level 0	Single Disk Storage	Single Disk Storage
CS Level 1	1132 Printer	SAC I/2250 or 1133 Multiplexer Control
CS Level 2		1132 Printer
CS Level 3		2501 Card Reader CPU

* 1130-B Logic pages have a machine designation of 1131-B
** 1130-C Logic pages have a machine designation of 1131-C

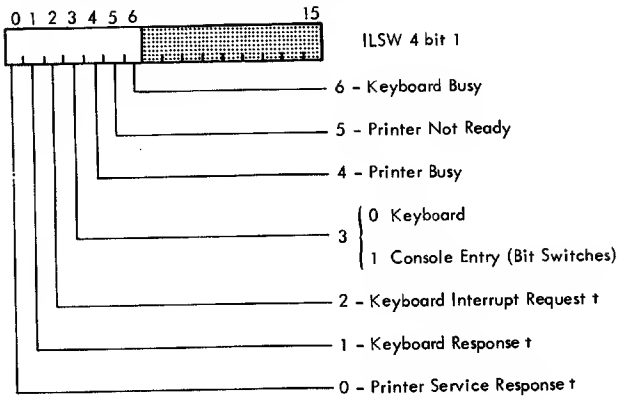
Figure 1-19. Cycle Steal Level Assignments

1133 Multiplexer Control Cycle Steol Priority Assignments		
MPX CS Level	0	2310 B Disk Storage Drive 1 or 2311 Disk Storage Drive 1
MPX CS Level	1	2310 B Disk Storage Drive 2 or 2311 Disk Storage Drive 2
MPX CS Level	2	2310 B Disk Storage Drive 3
MPX CS Level	3	2310 B Disk Storage Drive 4
MPX CS Level	4	
MPX CS Level	5	
MPX CS Level	6	SAC II
MPX CS Level	7	1403 Printer
MPX CS Level	8	Reserved for exponsion of the 1133 I/O devices.
MPX CS Level	9	
MPX CS Level	10	
MPX CS Level	11	

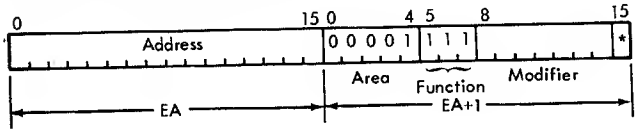
Note: All of the above MPX CS levels cause the 1133 Multiplexer Control to initiote o cycle steal level 1 request to the 1131 CPU.

Figure 1-20. 1133 Multiplexer Control Cycle Steal Priority Assignments

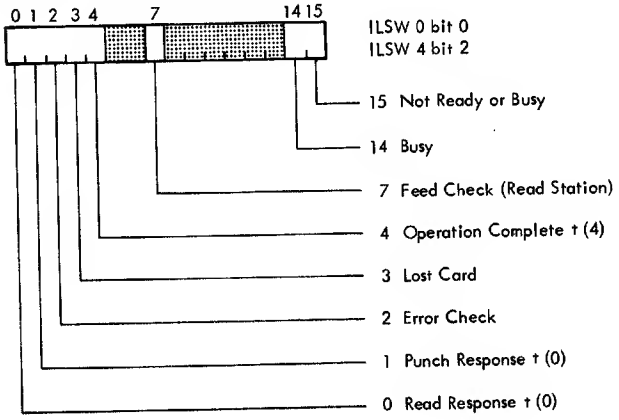
Console Printer/Keyboard Device Status Word



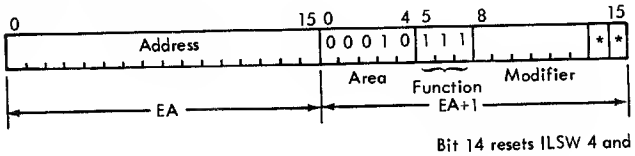
The Console Printer/Keyboard DSW is addressed by the following IOCC:



1442 Device Status Word



The 1442 Card Read Punch DSW is addressed by the following IOCC:

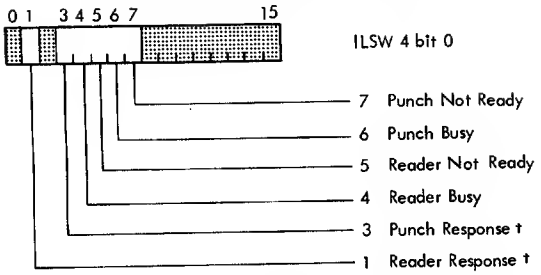


Bit 14 resets ILSW 4 and bit 15 resets ILSW 0

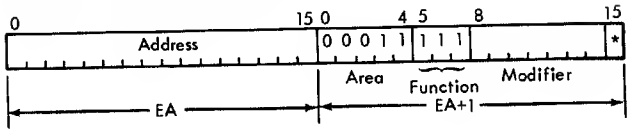
*If bit is a "1", the XIO sense DSW turns the associated ILSW indicator off.

† Sets associated ILSW bit.

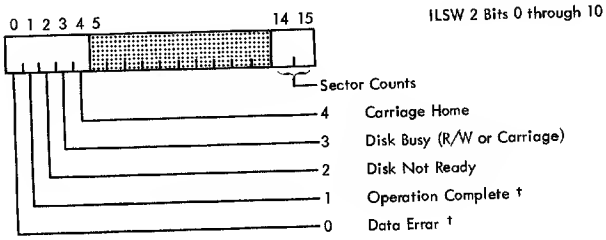
1134 and 1055 Device Status Word



The 1055 Paper Tape Punch and 1134 Paper Tape Reader DSW is addressed by the following IOCC:

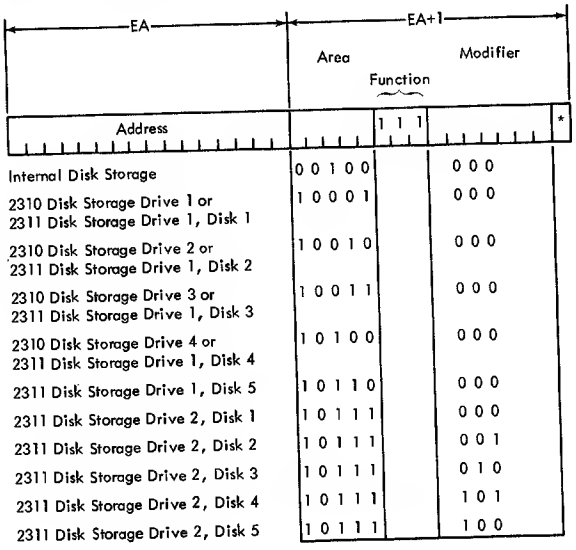


Disk Storage Status Word (Single Disk, 2310 and 2311)



† Sets associated ILSW bit.

The Basic Disk Storage, 2310, and 2311 Disk Storage DSW is addressed by the following IOCC's:

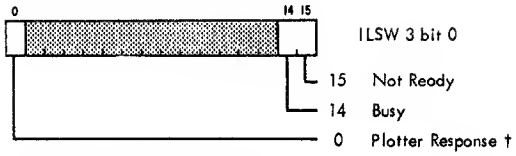


	Address		Modifier
Internal Disk Storage	0 0 1 0 0		0 0 0
2310 Disk Storage Drive 1 or 2311 Disk Storage Drive 1, Disk 1	1 0 0 0 1		0 0 0
2310 Disk Storage Drive 2 or 2311 Disk Storage Drive 1, Disk 2	1 0 0 1 0		0 0 0
2310 Disk Storage Drive 3 or 2311 Disk Storage Drive 1, Disk 3	1 0 0 1 1		0 0 0
2310 Disk Storage Drive 4 or 2311 Disk Storage Drive 1, Disk 4	1 0 1 0 0		0 0 0
2311 Disk Storage Drive 1, Disk 5	1 0 1 1 0		0 0 0
2311 Disk Storage Drive 2, Disk 1	1 0 1 1 1		0 0 0
2311 Disk Storage Drive 2, Disk 2	1 0 1 1 1		0 0 1
2311 Disk Storage Drive 2, Disk 3	1 0 1 1 1		0 1 0
2311 Disk Storage Drive 2, Disk 4	1 0 1 1 1		1 0 1
2311 Disk Storage Drive 2, Disk 5	1 0 1 1 1		1 0 0

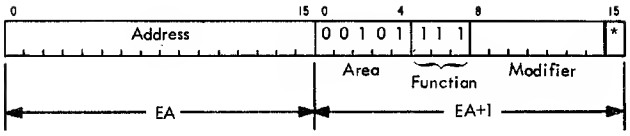
*If bit is a "1", the XIO sense DSW turns the associated ILSW indicator off.

Figure 1-21. Device Status Word Bit Assignments (Part 1)

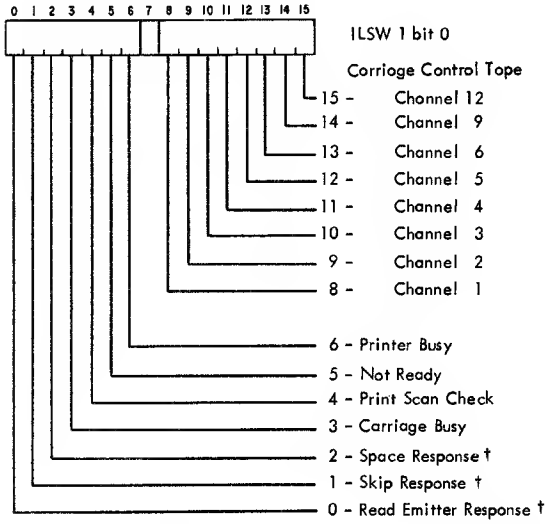
1627 Device Status Word



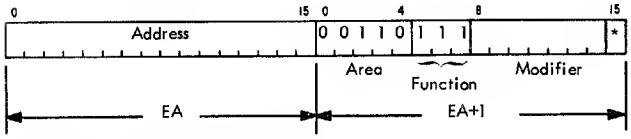
The 1627 Plotter DSW is addressed by the following IOCC:



1132 Device Status Word



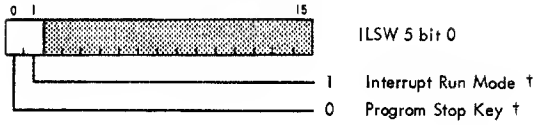
The 1132 Printer DSW is addressed by the following IOCC:



*If bit is a "1", the XIO sense DSW turns the associated ILSW indicator off.

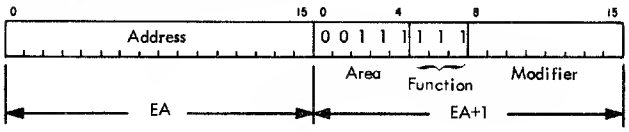
† Sets associated ILSW bit.

Program Stop Key and Interrupt Run Device Status Word

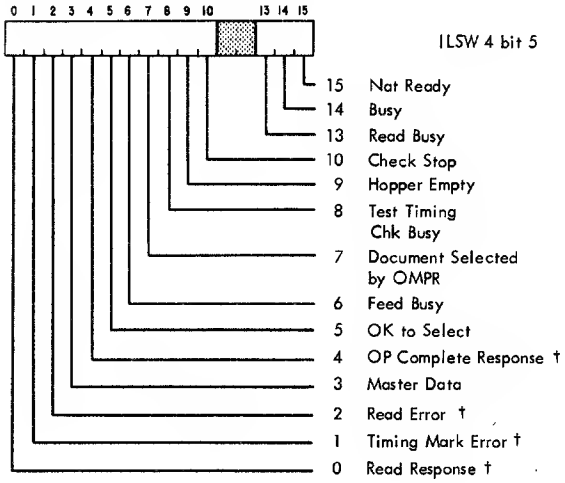


The Program Stop Key and Interrupt Run DSW is addressed by the following IOCC:

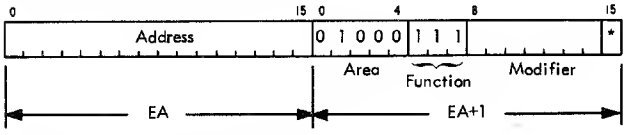
No ILSW Reset



1231 Device Status Word



The 1231 Optical Mark Page Reader DSW is addressed by the following IOCC:

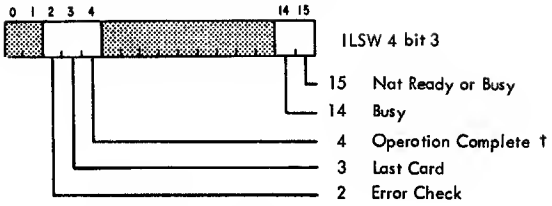


*If bit is a "1", the XIO sense DSW turns the associated ILSW indicator off.

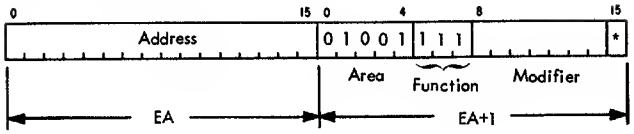
† Sets associated ILSW bit.

Figure 1-21. Device Status Word Bit Assignments (Part 2)

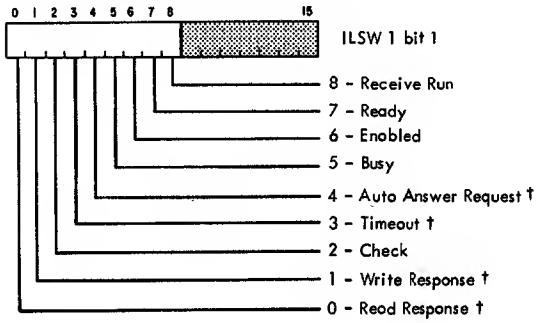
2501 Device Status Word



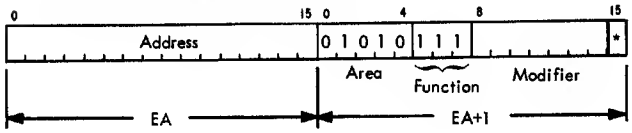
The 2501 Card Reader DSW is addressed by the following IOCC:



SCA Device Status Word



The Synchronous Communications Adapter DSW is addressed by the following IOCC:

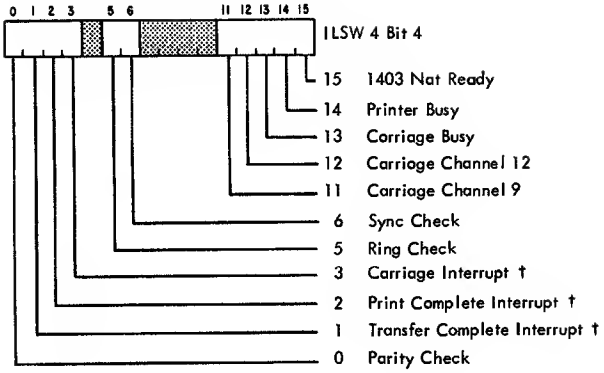


*If bit is a "1", the XIO sense DSW turns the associated ILSW indicator off.

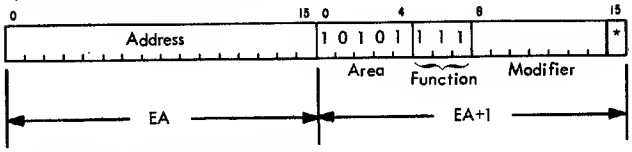
† Sets associated ILSW bit.

Figure 1-21. Device Status Word Bit Assignments (Part 3)

1403 Device Status Word



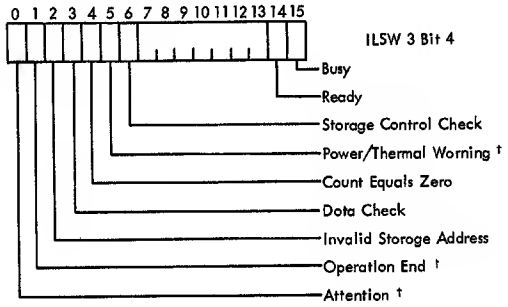
The 1403 Printer DSW is addressed by the following IOCC:



*If bit is a "1", the XIO sense DSW turns the associated ILSW indicator off.

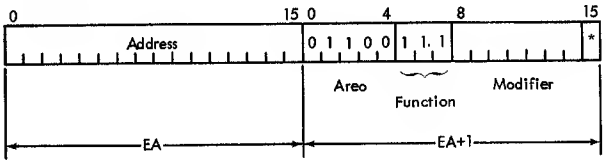
† Sets associated ILSW bit.

System/7 1130 Host Attachment Device Status Word



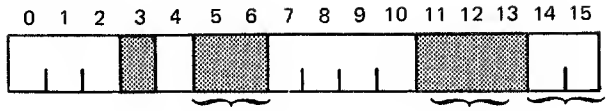
† Sets associated ILSW bit.

The System/7 1130 Host Attachment is addressed by the following IOCC:



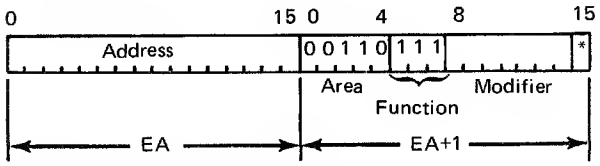
*If bit is a "1", the XIO sense DSW turns the associated ILSW indicator off.

2250 Device Status Word



14, 15	—	Address Displacement	Indicates number of locations the address register (in first word of read status response) is ahead of address of order being executed when Detect Interrupt occurred. Contains indeterminate value at any other time. Reset to 01.
11 - 13	—	Reserved (must be 0)	
10	—	Point Mode	Significant if bit 9 = 0; bit 10 = 1 for Point mode, or = 0 for Vector mode.
9	—	Character Mode	A 1 when in Basic or Large Character mode; 0 when in Graphic mode.
8	—	Busy	Display is currently regenerating in Cycle Steal mode. This bit is always 0 if interrupt has occurred and/or display is not regenerating.
7	—	Light Pen Switch Status	Light pen switch was closed when last Start Timer order was executed.
5, 6	—	Reserved (must be 0)	
4	—	Detect Status	Light pen has detected a point, vector, or character with interrupts deferred. This bit is reset whenever it is tested successfully or when DSW bit 2 is set.
3	—	Reserved (must be 0)	
2	—	Detect Interrupt	Light pen has detected a point vector, or character with interrupts enabled.
1	—	Keyboard Interrupt	A key has been pressed on either keyboard, and data is available.
0	—	Order Controlled Interrupt	Long Branch/Interrupt order caused the interrupt.

The 2250 Display Unit is addressed by the following IOCC:



*If bit is a "1", the XIO sense DSW turns the associated ILSW indicator off.

Figure 1-21. Device Status Word Bit Assignments (Part 4)

Core Storage Address (Decimal)	Use	Addressed By
0000	First Program Instruction	Program Start Key and M Register
0001	Index Register 1	Tag Bits = 01
0002	Index Register 2	Tag Bits = 10
0003	Index Register 3	Tag Bits = 11
0004-0007	General Usage	M Register
0008-0013	Interrupt Levels 0-5 Addresses	Wired Logic in Interrupt Circuits
0014-0031	General Usage; Used to Expand Interrupt Level Addresses on Some Special Machines	M Register or Wired Logic
0032-0039	Printer Scan Field	M Register

Figure 1-22. Reserved Core Storage Locations

Positive Binary Values Bit Positions 11 1111 0123 4567 8901 2345	Powers of 2	Absolute Values Decimal Notation Base-10	 Hexa-decimal Notation Base-16	Negative Binary Values Bit Positions 11 1111 0123 4567 8901 2345
0000 0000 0000 0000	-	0	0	No negative zero
0000 0000 0000 0001	0	1	1	1111 1111 1111 1111
0000 0000 0000 0010	1	2	2	1111 1111 1111 1110
0000 0000 0000 0100	2	4	4	1111 1111 1111 1100
0000 0000 0000 1000	3	8	8	1111 1111 1111 1000
0000 0000 0001 0000	4	16	10	1111 1111 1111 0000
0000 0000 0010 0000	5	32	20	1111 1111 1110 0000
0000 0000 0100 0000	6	64	40	1111 1111 1100 0000
0000 0000 1000 0000	7	128	80	1111 1111 1000 0000
0000 0001 0000 0000	8	256	100	1111 1111 0000 0000
0000 0010 0000 0000	9	512	200	1111 1110 0000 0000
0000 0100 0000 0000	10	1,024	400	1111 1100 0000 0000
0000 1000 0000 0000	11	2,048	800	1111 1000 0000 0000
0001 0000 0000 0000	12	4,096	1,000	1111 0000 0000 0000
0010 0000 0000 0000	13	8,192	2,000	1110 0000 0000 0000
0100 0000 0000 0000	14	16,384	4,000	1100 0000 0000 0000
0111 1111 1111 1111	-	32,767	7,FFF	1000 0000 0000 0001
No positive equivolent	15	32,768	8,000	1000 0000 0000 0000

Figure 1-23. Value Ranges - Single Precision Word

Positive Binary Values Bit Positions 11 1111 1111 2222 2222 2233 0123 4567 8901 2345 6789 0123 4567 8901	Powers of 2	Absolute Values Decimal Notation Base - 10	 Hexadecimal Notation Base - 16	Negative Binary Values Bit Positions 11 1111 1111 2222 2222 2233 0123 4567 8901 2345 6789 0123 4567 8901
0000 0000 0000 0000 0000 0000 0000 0000	-	0	0	No negative zero
0000 0000 0000 0000 0000 0000 0000 0001	0	1	1	1111 1111 1111 1111 1111 1111 1111 1111
0000 0000 0000 0000 0000 0000 0000 0010	1	2	2	1111 1111 1111 1111 1111 1111 1111 1110
0000 0000 0000 0000 0000 0000 0000 0100	2	4	4	1111 1111 1111 1111 1111 1111 1111 1100
0000 0000 0000 0000 0000 0000 0000 1000	3	8	8	1111 1111 1111 1111 1111 1111 1111 1000
0000 0000 0000 0000 0000 0000 0001 0000	4	16	10	1111 1111 1111 1111 1111 1111 1111 0000
0000 0000 0000 0000 0000 0000 0010 0000	5	32	20	1111 1111 1111 1111 1111 1111 1110 0000
0000 0000 0000 0000 0000 0000 0100 0000	6	64	40	1111 1111 1111 1111 1111 1111 1100 0000
0000 0000 0000 0000 0000 0000 1000 0000	7	128	80	1111 1111 1111 1111 1111 1111 1000 0000
0000 0000 0000 0000 0000 0001 0000 0000	8	256	100	1111 1111 1111 1111 1111 1111 0000 0000
0000 0000 0000 0000 0000 0010 0000 0000	9	512	200	1111 1111 1111 1111 1111 1110 0000 0000
0000 0000 0000 0000 0000 0100 0000 0000	10	1,024	400	1111 1111 1111 1111 1111 1100 0000 0000
0000 0000 0000 0000 0000 1000 0000 0000	11	2,048	800	1111 1111 1111 1111 1111 1000 0000 0000
0000 0000 0000 0000 0001 0000 0000 0000	12	4,096	1,000	1111 1111 1111 1111 1111 0000 0000 0000
0000 0000 0000 0000 0010 0000 0000 0000	13	8,192	2,000	1111 1111 1111 1111 1110 0000 0000 0000
0000 0000 0000 0000 0100 0000 0000 0000	14	16,384	4,000	1111 1111 1111 1111 1100 0000 0000 0000
0000 0000 0000 0000 1000 0000 0000 0000	15	32,768	8,000	1111 1111 1111 1111 1000 0000 0000 0000
0000 0000 0000 0001 0000 0000 0000 0000	16	65,536	10,000	1111 1111 1111 1111 0000 0000 0000 0000
0000 0000 0000 0010 0000 0000 0000 0000	17	131,072	20,000	1111 1111 1111 1110 0000 0000 0000 0000
0000 0000 0000 0100 0000 0000 0000 0000	18	262,144	40,000	1111 1111 1111 1100 0000 0000 0000 0000
0000 0000 0000 1000 0000 0000 0000 0000	19	524,288	80,000	1111 1111 1111 1000 0000 0000 0000 0000
0000 0000 0001 0000 0000 0000 0000 0000	20	1,048,576	100,000	1111 1111 1111 0000 0000 0000 0000 0000
0000 0000 0010 0000 0000 0000 0000 0000	21	2,097,152	200,000	1111 1111 1110 0000 0000 0000 0000 0000
0000 0000 0100 0000 0000 0000 0000 0000	22	4,194,304	400,000	1111 1111 1100 0000 0000 0000 0000 0000
0000 0000 1000 0000 0000 0000 0000 0000	23	8,388,608	800,000	1111 1111 1000 0000 0000 0000 0000 0000
0000 0001 0000 0000 0000 0000 0000 0000	24	16,777,216	1,000,000	1111 1111 0000 0000 0000 0000 0000 0000
0000 0010 0000 0000 0000 0000 0000 0000	25	33,554,432	2,000,000	1111 1110 0000 0000 0000 0000 0000 0000
0000 0100 0000 0000 0000 0000 0000 0000	26	67,108,864	4,000,000	1111 1100 0000 0000 0000 0000 0000 0000
0000 1000 0000 0000 0000 0000 0000 0000	27	134,217,728	8,000,000	1111 1000 0000 0000 0000 0000 0000 0000
0001 0000 0000 0000 0000 0000 0000 0000	28	268,435,456	10,000,000	1111 0000 0000 0000 0000 0000 0000 0000
0010 0000 0000 0000 0000 0000 0000 0000	29	536,870,912	20,000,000	1110 0000 0000 0000 0000 0000 0000 0000
0100 0000 0000 0000 0000 0000 0000 0000	30	1,073,741,824	40,000,000	1100 0000 0000 0000 0000 0000 0000 0000
0111 1111 1111 1111 1111 1111 1111 1111	-	2,147,483,647	7F,FFF,FFF	1000 0000 0000 0000 0000 0000 0000 0001
No positive equivolent	31	2,147,483,648	80,000,000	1000 0000 0000 0000 0000 0000 0000 0000

Figure 1-24. Value Ranges - Double Precision Word

Character	Hex	I/O Bus Bits							
		0	1	2	3	4	5	6	7
A	C1	1	1	0	0	0	0	0	1
B	C2	1	1	0	0	0	0	1	0
C	C3	1	1	0	0	0	0	1	1
D	C4	1	1	0	0	0	1	0	0
E	C5	1	1	0	0	0	1	0	1
F	C6	1	1	0	0	0	1	1	0
G	C7	1	1	0	0	0	1	1	1
H	C8	1	1	0	0	1	0	0	0
I	C9	1	1	0	0	1	0	0	1
J	D1	1	1	0	1	0	0	0	1
K	D2	1	1	0	1	0	0	1	0
L	D3	1	1	0	1	0	0	1	1
M	D4	1	1	0	1	0	1	0	0
N	D5	1	1	0	1	0	1	0	1
O	D6	1	1	0	1	0	1	1	0
P	D7	1	1	0	1	0	1	1	1
Q	D8	1	1	0	1	1	0	0	0
R	D9	1	1	0	1	1	0	0	1
S	E2	1	1	1	0	0	0	1	0
T	E3	1	1	1	0	0	0	1	1
U	E4	1	1	1	0	0	1	0	0
V	E5	1	1	1	0	0	1	0	1
W	E6	1	1	1	0	0	1	1	0
X	E7	1	1	1	0	0	1	1	1
Y	E8	1	1	1	0	1	0	0	0
Z	E9	1	1	1	0	1	0	0	1
0	F0	1	1	1	1	0	0	0	0
1	F1	1	1	1	1	0	0	0	1
2	F2	1	1	1	1	0	0	1	0
3	F3	1	1	1	1	0	0	1	1
4	F4	1	1	1	1	0	1	0	0
5	F5	1	1	1	1	0	1	0	1
6	F6	1	1	1	1	0	1	1	0
7	F7	1	1	1	1	0	1	1	1
8	F8	1	1	1	1	1	0	0	0
9	F9	1	1	1	1	1	0	0	1
=	7E	0	1	1	1	1	1	1	0
$	5B	0	1	0	1	1	0	1	1
.	4B	0	1	0	0	1	0	1	1
'	7D	0	1	1	1	1	1	0	1
,	6B	0	1	1	0	1	0	1	1
(	4D	0	1	0	0	1	1	0	1
-	60	0	1	1	0	0	0	0	0
)	5D	0	1	0	1	1	1	0	1
+	4E	0	1	0	0	1	1	1	0
/	61	0	1	1	0	0	0	0	1
*	5C	0	1	0	1	1	1	0	0
&	50	0	1	0	1	0	0	0	0

Figure 1-25. 1132 Printer Code

Character	Hex	Bits							
		0	1	2	3	4	5	6	7
		8	9	10	11	12	13	14	15
A	64	0	1	1	0	0	1	0	0
B	25	0	0	1	0	0	1	0	1
C	26	0	0	1	0	0	1	1	0
D	67	0	1	1	0	0	1	1	1
E	68	0	1	1	0	1	0	0	0
F	29	0	0	1	0	1	0	0	1
G	2A	0	0	1	0	1	0	1	0
H	6B	0	1	1	0	1	0	1	1
I	2C	0	0	1	0	1	1	0	0
J	58	0	1	0	1	1	0	0	0
K	19	0	0	0	1	1	0	0	1
L	1A	0	0	0	1	1	0	1	0
M	5B	0	1	0	1	1	0	1	1
N	1C	0	0	0	1	1	1	0	0
O	5D	0	1	0	1	1	1	0	1
P	5E	0	1	0	1	1	1	1	0
Q	1F	0	0	0	1	1	1	1	1
R	20	0	0	1	0	0	0	0	0
S	0D	0	0	0	0	1	1	0	1
T	0E	0	0	0	0	1	1	1	0
U	4F	0	1	0	0	1	1	1	1
V	10	0	0	0	1	0	0	0	0
W	51	0	1	0	1	0	0	0	1
X	52	0	1	0	1	0	0	1	0
Y	13	0	0	0	1	0	0	1	1
Z	54	0	1	0	1	0	1	0	0
0	49	0	1	0	0	1	0	0	1
1	40	0	1	0	0	0	0	0	0
2	01	0	0	0	0	0	0	0	1
3	02	0	0	0	0	0	0	1	0
4	43	0	1	0	0	0	0	1	1
5	04	0	0	0	0	0	1	0	0
6	45	0	1	0	0	0	1	0	1
7	46	0	1	0	0	0	1	1	0
8	07	0	0	0	0	0	1	1	1
9	08	0	0	0	0	1	0	0	0
=	4A	0	1	0	0	1	0	1	0
$	62	0	1	1	0	0	0	1	0
.	6E	0	1	1	0	1	1	1	0
'	0B	0	0	0	0	1	0	1	1
,	16	0	0	0	1	0	1	1	0
(	57	0	1	0	1	0	1	1	1
-	61	0	1	1	0	0	0	0	1
)	2F	0	0	1	0	1	1	1	1
+	6D	0	1	1	0	1	1	0	1
/	4C	0	1	0	0	1	1	0	0
*	23	0	0	1	0	0	0	1	1
&	15	0	0	0	1	0	1	0	1
Blank	7F	0	1	1	1	1	1	1	1

Figure 1-26. 1403 Printer Code

Console Printer Control Codes	
Function	0 1 2 3 4 5 6 7 8 15
Carrier Return	1 0 0 0 0 0 0 1
Tabulate	0 1 0 0 0 0 0 1
Space	0 0 1 0 0 0 0 1
Backspace	0 0 0 1 0 0 0 1
Shift to Red*	0 0 0 0 1 0 0 1
Shift to Black*	0 0 0 0 0 1 0 1
Line Feed	0 0 0 0 0 0 1 1

*May be done concurrently with any other function.

Console Printer Character Codes								
Character Code Bits						U/L Case		Ctrl
B0	B1	B2	B3	B4	B5	B6=0 LC	B6=1 UC	B7
0	0	1	1	1	1	A	A	0
0	0	0	1	1	0	B	B	0
0	0	0	1	1	1	C	C	0
0	0	1	1	0	0	D	D	0
0	0	1	1	0	1	E	E	0
0	0	0	1	0	0	F	F	0
0	0	0	1	0	1	G	G	0
0	0	1	0	0	1	H	H	0
0	0	1	0	0	0	I	I	0
0	1	1	1	1	1	J	J	0
0	1	0	1	1	0	K	K	0
0	1	0	1	1	1	L	L	0
0	1	1	1	0	0	M	M	0
0	1	1	1	0	1	N	N	0
0	1	0	1	0	0	O	O	0
0	1	0	1	0	1	P	P	0
0	1	1	0	0	1	Q	Q	0
0	1	1	0	0	0	R	R	0
1	0	0	1	1	0	S	S	0
1	0	0	1	1	1	T	T	0
1	0	1	1	0	0	U	U	0
1	0	1	1	0	1	V	V	0
1	0	0	1	0	0	W	W	0
1	0	0	1	0	1	X	X	0
1	0	1	0	0	1	Y	Y	0
1	0	1	0	0	0	Z	Z	0
1	1	1	1	1	1	1	(	0
1	1	0	1	1	0	2	+	0
1	1	0	1	1	1	3	<	0
1	1	1	1	0	0	4	¬	0
1	1	1	1	0	1	5	)	0
1	1	0	1	0	0	6	;	0
1	1	0	1	0	1	7	*	0
1	1	1	0	0	1	8	'	0
1	1	1	0	0	0	9	"	0
1	1	0	0	0	1	0	|	0
1	1	0	0	0	0	#	=	0
1	0	1	1	1	1	/	–	0
1	0	0	0	0	1	-	?	0
1	0	0	0	0	0	,	:	0
0	1	0	0	0	1	&	>	0
0	1	0	0	0	0	$	.	0
0	0	0	0	0	1	@	%	0
0	0	0	0	0	0	.	¢	0

Console Keyboard Character Codes																	
Key	1BM Card Code	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
*	11,8,4		1					1				1					
/	0,1			1	1												
Ø	0			1													
1	1				1												
2	2					1											
3	3						1										
4	4							1									
5	5								1								
6	6									1							
7	7										1						
8	8											1					
9	9												1				
$	11,8,3		1				1					1					
.	12,8,3	1					1					1					
	0,8,3			1			1					1					
EOF	None													1			
Back Space	None														1		
ER FLD	None															1	
=	6,8									1		1					
'	5,8								1			1					
(	12,5,8	1						1				1					
)	11,5,8		1						1			1					
+	12,8,6	1								1		1					
-	11		1														
A	12,1	1			1												
B	12,2	1				1											
C	12,3	1					1										
D	12,4	1						1									
E	12,5	1							1								
F	12,6	1								1							
G	12,7	1									1						
H	12,8	1										1					
I	12,9	1											1				
J	11,1		1		1												
K	11,2		1			1											
L	11,3		1				1										
M	11,4		1					1									
N	11,5		1						1								
O	11,6		1							1							
P	11,7		1								1						
Q	11,8		1									1					
R	11,9		1										1				
S	0,2			1		1											
T	0,3			1			1										
U	0,4			1				1									
V	0,5			1					1								
W	0,6			1						1							
X	0,7			1							1						
Y	0,8			1								1					
Z	0,9			1									1				
Space	Blank	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
¢	12,8,2	1				1						1					
<	12,8,4	1						1				1					
|	12,8,7	1									1	1					
&	12	1															
[	11,8,2		1			1						1					
;	11,8,6		1							1		1					
¬	11,8,7		1								1	1					
%	0,8,4			1				1				1					
-	0,8,5			1					1			1					
>	0,8,6			1						1		1					
?	0,8,7			1							1	1					
:	8,2					1						1					
#	8,3						1					1					
@	8,4							1				1					
"	8,7										1	1					

Figure 1-27. Console Printer and Keyboard Reference Charts

STR Control Sequence	Control Character Sequence	
	Leader Character	Trailer Character
End of IDLE (EOI)*	CL	1_6IDLE
Inquiry (Synchronized ?)*	TL	INQ
Acknowledge (Synchronized)	CL	ACK 2
Telephone Sequence *	CL	TEL
Acknowledge Telephone *	CL	TEL
Start of Record 1 (SOR 1) 1st or odd numbered record	TL	SOR 1
Start of Record 2 (SOR 2) 2nd or even numbered record	TL	SOR 2
End of Transmittal Record (EOTR)	TL	LRC
Acknowledge Record 1	CL	ACK 1
Acknowledge Record 2	CL	ACK 2
Repeat Last Record (ERROR)	CL	ERR
Intermediate LRC**	GM	LRC
End of Transmission (EOT)*	CL	EOT
Acknowledge EOT *	CL	EOT

*These sequences are always preceded by a 1.25 second transmission of IDLE characters.
** This sequence may be required on some terminals i.e. 1013, 7701, 7702

STR Control Chorocters	4 of 8 Code								
	N	X	O	R	8	4	2	1	Hex
Idle	0	0	1	1	1	0	0	1	39
Start of Record 1 or Acknowledge 1 (SOR 1 or ACK 1)	0	1	0	1	0	0	1	1	53
Start of Record 2 or Acknowledge 2 (SOR 2 or ACK 2)	0	0	1	1	0	0	1	1	33
Transmit Leader (TL)	0	0	1	1	0	1	0	1	35
Control Leader (CL)	0	1	0	1	0	1	0	1	55
End of Transmission (EOT) *	0	1	0	1	1	0	1	0	5A
Inquiry or Error (iNQ or ERR)	0	1	0	1	1	0	0	1	59
Telephone *	0	1	0	1	1	1	0	0	5C
Group Mark	1	0	0	0	1	1	0	1	8D
Longitudinal Redundancy Check (LRC) **	-	-	-	-	-	-	-	-	

* Also used as a data character
** The LRC character contains a 1 in each bit position for which the total of 1's in the record was odd, and a 0 if the total was even. The character is not necessarily in the 4 of 8 code.

STR 4-of-8 Transmission Codes

Graphic	4 of 8 Code NXOR 8421	Hex	Graphic	4 of 8 Code NXOR 8421	Hex
blank	1111 0000 ①	F0	F	0110 0110	66
¢	0110 1010	6A	G	1000 0111	87
.	1000 1011	8B	H	0111 1000	78
<	0110 1100	6C	I	0110 1001	69
(	0101 0110	56	J	1101 0001	D1
+	0011 0110	36	K	1101 0010	D2
| ②	1000 1101	8D	L	1100 0011	C3
&	1000 1110	8E	M	1101 0100	D4
!	1100 1010	CA	N	1100 0101	C5
$	0100 1011	4B	O	1100 0110	C6
*	1100 1100	CC	P	0100 0111	47
)	0101 1100	5C	Q	1101 1000	D8
;	0011 1100	3C	R	1100 1001	C9
¬	0100 1101	4D	none ③	1010 1010	AA
-	0100 1110	4E	S	1011 0010	B2
/	1011 0001	B1	T	1010 0011	A3
,	0010 1011	2B	U	1011 0100	B4
%	1010 1100	AC	V	1010 0101	A5
—	0101 1010	5A	W	1010 0110	A6
>	0011 1010	3A	X	0010 0111	27
?	0010 1101	2D	Y	1011 1000	B8
:	0010 1110 ①	2E	Z	1010 1001	A9
#	0001 1011	1B	0	1001 1010	9A
@	1001 1100	9C	1	1110 0001	E1
'	0000 1111	0F	2	1110 0010	E2
=	0001 1110	1E	3	1001 0011	93
"	0001 1101	1D	4	1110 0100	E4
A	0111 0001	71	5	1001 0101	95
B	0111 0010	72	6	1001 0110	96
C	0110 0011	63	7	0001 0111	17
D	0111 0100	74	8	1110 1000	E8
E	0110 0101	65	9	1001 1001	99

①This is correct for System/360 Programs, but is not consistent with certain other STR devices. See the specific device manual.
②Group Mark
③Record Mark

Figure 1-28. Synchronous Communications Adapter Reference Charts (Part 1)

BSC CONTROL CHARACTERS			
Character	Bit Configuration 0 1 2 3 4 5 6 7	Hex	Meaning
SYN	0 0 1 1 0 0 1 0	32	Synchronous Idle
DLE	0 0 0 1 0 0 0 0	10	Data Link Escape
ENQ	0 0 1 0 1 1 0 1	2D	Enquiry
SOH	0 0 0 0 0 0 0 1	01	Start of Heading
STX	0 0 0 0 0 0 1 0	02	Start of Text
ETB	0 0 1 0 0 1 1 0	26	End of Transmission Block
ETX	0 0 0 0 0 0 1 1	03	End of Text
EOT	0 0 1 1 0 1 1 1	37	End of Transmission
NAK	0 0 1 1 1 1 0 1	3D	Negative Acknowledgement
* ACK 0	0 1 1 1 0 0 0 0	70	Positive Acknowledgement (even record)
* ACK 1	0 1 1 0 0 0 0 1	61	Positive Acknowledgement (odd record)
WACK	0 1 1 0 1 0 1 1	6B	Wait before ACK
ITB	0 0 0 1 1 1 1 1	1F	End of Intermediate Transmission Block

* Control characters when preceded by DLE

BSC CONTROL SEQUENCES	
Characters	Meaning
ENQ	Enquiry
SOH	Start of Heading
STX	Start of Text
DLE STX	Start of Transparent Test
ETB CRC-16 *	End of Block
DLE ETB CRC-16	End of Transparent Block
ETX CRC-16	End of Text
DLE ETX CRC-16	End of Transparent Text
DLE ACK 1	Acknowledgement of Odd Record
DLE ACK 0	Acknowledgement of Even Record
NAK	Negative Acknowledgement
EOT	End of Transmission
DLE EOT	Disconnect Signal
SYN SYN	Synchronous Idle (Normal)
DLE SYN	Synchronous Idle (Transparent Text)

* CRC-16 is a 16-bit cyclic check character accumulated from text and heading data.

TRANSMISSION TIMING			
Time Between Characters			
Baud \ Char. Size	6 Bit	7 Bit	8 Bit
600	10.0 ms	11.6 ms	13.3 ms
1200	5.0 ms	5.8 ms	6.6 ms
2000	3.0 ms	3.5 ms	4.0 ms
2400	2.5 ms	2.9 ms	3.3 ms
4800	1.25 ms	1.45 ms	1.65 ms
Character Rate			
Baud \ Char. Size	6 Bit	7 Bit	8 Bit
600	100 cps	85.7 cps	75 cps
1200	200 cps	171 cps	150 cps
2000	333.3 cps	286 cps	250 cps
2400	400 cps	343 cps	300 cps
4800	800 cps	686 cps	600 cps

Figure 1-28. Synchronous Communications Adapter Reference Charts (Part 2)

2250 Display Unit Order Formats

Orders	Bit Positions															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Short Branch	0	0	0	4096	2048	1024	512	256	128	Address 64	32	16	8	4	2	1
Long Branch Interrupt	0	0	1	0	0 = Int 1 = Br	No Op			Indirect Address						LP Det Cond	LP SW Cond
	Address															
Set Pen Mode	0	0	1	1	0	0	0	1		Note 1	Note 2	Enable LP Det	Disable LP Det	Enable LP Det Int	Defer LP Det Int	
Set Graphic Mode	0	0	1	1	0	0	1	0							0=Vector 1=Point	
Set Char. Mode	0	0	1	1	0	0	1	1							0=Small 1=Large	
Start Regen Timer	0	0	1	1	0	1	0	0								
Store Revert Register	0	0	1	1	0	1	0	1								
	Revert register is stored in this word.															
Revert	0	0	1	1	0	1	1	0								
No Op	0	0	1	1	0	0	0	1								
Long Absolute Position	0	1	0	Beam on if 1			512	256	128	64	X Coordinate 32	16	8	4	2	1
							Y Coordinate									
Short Absolute	0	1	1	Beam on if 1	0 = X 1 = Y		X or Y Coordinate									
Incremental	1	Sign of X	32	16	X Increment* 8	4	2	1	Beam on if 1	Sign of Y	32	16	Y Increment* 8	4	2	1
Character Strokes	0 = Short 1 = Long	Stroke Xa			Beam (a) on if 1	Stroke Ya			Revert	Stroke Xb			Beam (b) on if 1	Stroke Yb		
Subscript		1	1	1		0	0	1	Revert							
Null		1	1	1		0	1	0	1							
Superscript		1	1	1		1	0	0	Revert							
New Line		1	1	1		1	1	1	1							
No Op		1	1	1		0	1	0	0							

* Negative increments must be in two's complement form.

Note 1: Diagnostic Set LP Detect Status
Note 2: Diagnostic Set LP Sw Active Latch

Figure 1-29. 2250 Display Unit Reference Charts (Part 1)

2250 Display Unit Order Mnemonics

Mnemonic	Function	Mnemonic	Function
CS	Control Stroke	MBA	Move Beam Absolute
DBA	Draw Beam Absolute	MBAX	Move Beam Absolute X
DBAX	Draw Beam Absolute X	MBAY	Move Beam Absolute Y
DBAY	Draw Beam Absolute Y	MBI	Move Beam Incremental
DBI	Draw Beam Incremental	MBS	Move Beam Stroke
DBS	Draw Beam Stroke	RVT	Revert
GB	Graphic Branch	SRVT	Save Revert Register
GBC	Graphic Branch Conditional	SCMB	Set Character Mode Basic
GBCE	Graphic Branch Cond External	SCML	Set Character Mode Large
GBE	Graphic Branch External	SGMP	Set Graphic Mode Point
GI	Graphic Interrupt	SGMV	Set Graphic Mode Vector
GIC	Graphic Interrupt Conditional	SPM	Set Pen Mode
GNOP	Graphic No-Operation	STMR	Start Regeneration Timer
GSB	Graphic Short Branch		

Figure 1-29. 2250 Display Unit Reference Charts (Part 2)

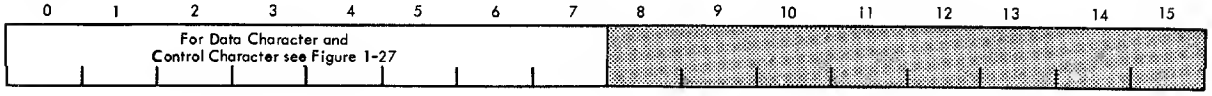
Description of Charts

IOCC control word is given in hexadecimal form with function modifier shown when applicable. Control word is followed by functional description and data word(s). Control words given are for device area codes. C(IOCC address) = core storage location specified by IOCC address. For all areas, Sense Interrupt command is 03XX; modifier XX (ILSW address) is placed on Out Bus automatically by the CPU.

Printer - Keyboard

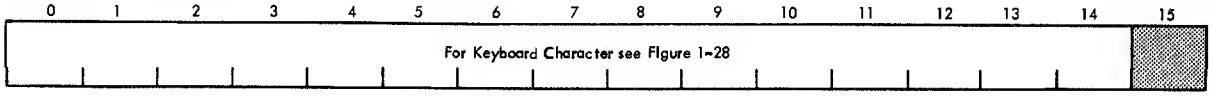
0900 Write: Load adapter buffer from C(IOCC address), analyze data, and send character signals to printer.

Data Word



0A00 Read: Store contents of keyboard contacts at C(IOCC address).

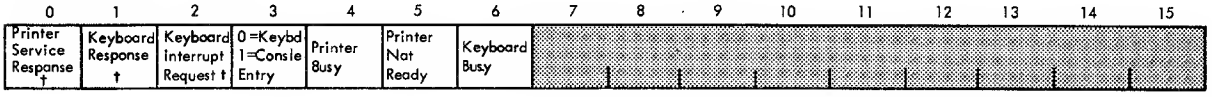
Data Word



0C00 Control: Places the keyboard in the select mode and allows data to be entered into the CPU.

0F00/0F01 Sense DSW: Loads device status indicators into A. Indicators (†) are reset by command 0F01.

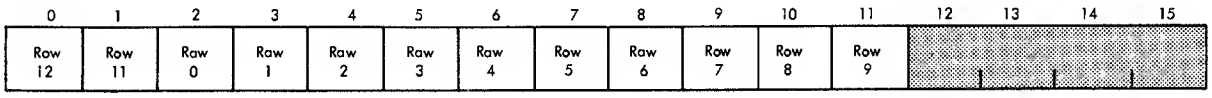
Device Status Word



1442 Card Read Punch

1100 Write: Load adapter buffer from C(IOCC address), and send character signals to punch. Cards are punched one column at a time.

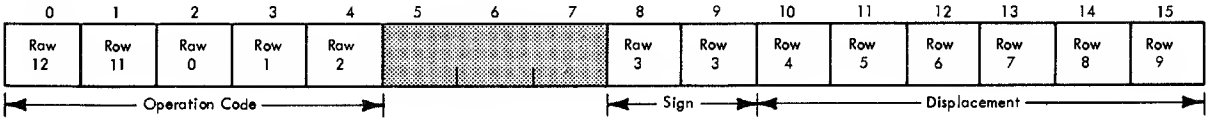
Data Word



1200 Read: Store contents of adapter buffer at C(IOCC address). Data word is same as for write.

Program Load Mode Read: This read is initialsed by the program load pushbutton. The data is read from the cards as shown below.

Data Word



1401 Cantral, Start Punch: Causes a card to move through the punch station and allows each column to generate a punch response interrupt.

1402 Control, Feed Cycle: Causes all cards in the feed path to advance one station. The read response and punch response interrupts are inhibited.

1404 Control, Start Read: Causes a card to move through the read station and allows each column to generate a read response interrupt.

148X Cantral, Stacker Select: Causes the card leaving the punch area to go to the alternate stacker. This command can be 1481, 1482, or 1484.

Figure 1-30. XIO Operations (Part 1)

1442 Card Read Punch - Continued

1700/1701 Sense Device: Loads the device status indicators into A. Command 1701 resets the interrupt level 0 indicators, and 1702 resets the interrupt level 4 indicators.

Device Status Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Read Response Level 0 †	Punch Response Level 0 †	Error Check	Last Card	Op Complete Level 4 †			Feed Check							Busy	Not Ready or Busy

1134 Paper Tape Reader and 1055 Paper Tape Punch

1900 Write: Load adapter punch buffer from C(IOCC address). Select punch magnet drivers from punch buffer data and energize punch clutch driver.

Data Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Channel 8	Channel 7	Channel 6	Channel 5	Channel 4	Channel 3	Channel 2	Channel 1								

1A00 Read: Store contents of adapter read buffer at C(IOCC address). Data word is same as for Write command.

Program Load Mode Read: This read is initiated by the Program Load pushbutton when a 1442 or 2501 card reader is not used with the 1131. The data is read from the tape as shown below:

Data Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Channel 4	Channel 3	Channel 2	Channel 1	Channel 4	Channel 3	Channel 2	Channel 1	Channel 4	Channel 3	Channel 2	Channel 1	Channel 4	Channel 3	Channel 2	Channel 1
← 1st Tape Character →				← 2nd Tape Character →				← 3rd Tape Character →				← 4th Tape Character →			

1C00 Control: Load contents of tape sensing contacts into adapter read buffer. Energizes reader clutch to advance tape one character position. IOCC address word is not used.

1F00 / 1F01 Sense Device: Load status of device indicators into A. Indicators (†) are reset by 1F01 command only.

Device Status Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	Reader Response †		Punch Response †	Reader Busy	Reader Not Ready	Punch Busy	Punch Not Ready								

Disk Storage (Single Disk, 2310, and 2311)

8C00/8C04
9400/9404
9C00/9C04
A400/A404
B400/B404
BC00/BC04

Control Carriage: Load IOCC address into adapter word counter to specify number of cylinders to be accessed. XX00 commands move the carriage forward. XX04 commands move the carriage in reverse.

IOCC Address Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
							Number of Cylinders								
							256	128	64	32	16	8	4	2	1

Figure 1-30. XIO Operations (Part 2)

Disk Storage (Single Disk, 2310, and 2311) - Continued

8D0X
950X
9D0X
A50X
B50X
8D0X

Initialize Write: Set up adapter data channel controls for transferring data from core storage to the adapter an a cycle-steol bosis.
Load IOCC address word into CAR.
Bit 13 determines the head, 0 for upper head, 1 far lawer heod.
Bits 14 and 15 determine the sector.
X=0, 1, 2, or 3; upper head, sector 1 thraugh 4 respectively.
X=4, 5, 6 ar 7; lawer head, sector 1 thraugh 4 respectively.

8E0X
960X
9E0X
A60X
B60X
BE0X

Initialize Read: Set up adapter data channel controls for transferring data fram the adapter to core storage on a cycle-steal basis. Load IOCC address ward into CAR. Word-count ward and data ward are same as for Initialize Write cammand.

X Same as the Initialize Write cammands.

8F00/8F01
9700/8701
9F00/9F01
A700/A701
B700/B701
BF00/BF01

Sense Device: Laad status of device indicators into A. Indicators (†) are reset by XX01 cammand.

Nate: I/O device/functian codes BCXX, BDXX, BEXX and BFXX require the use of modifier bits 9, 10, and 11 ta select the desired disk on the 2311 disk drive 2. Disks 3 and 4 are nat used if the 2311 is a model 12.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Data Errar †	Opera-tion Cam-plete †	Disk Nat Ready	Disk Busy R/W or Carriage	Carriage Home										Sector Count	

† Causes interrupt bit to be set in the ILSW.

1627 Plotter

2900 Write: Load adapter buffer fram C(IOCC address). Actuate platter cantrals fram buffer data.

Data Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Lower Pen	+X	-X	-Y	+Y	Raise Pen										

2F00/2F01 Sense Device: Load status of device indicotars into A. Indicators (†) are reset by 2F01 command only.

Device Status Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Platter Response †														Busy	Not Ready

1132 Printer

3200 Read Emitter: Causes the read emitter to transfer the next available type wheel character to C(IOCC address).

Data Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit 0 Row	Bit 1 Raw	Bit 2 Row	Bit 3 Raw	Bit 4 Raw	Bit 5 Raw	Bit 6 Raw	Bit 7 Row								

Figure 1-30. XIO Operations (Part 3)

1132 Printer - Continued

3401 Control, Space Carriage: Causes the carriage to space one line.

3402 Control, Stop Carriage: Causes the carriage to stop skipping on the detection of a punch in the carriage control tape.

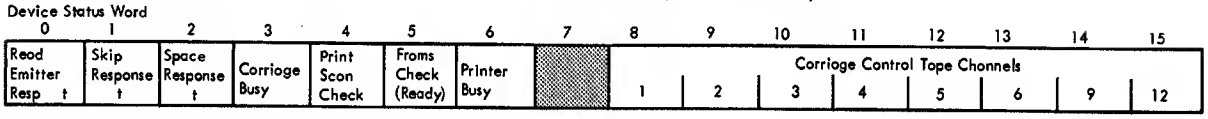
3404 Control, Start Carriage: Causes the carriage to skip until a punch is detected in the carriage control tape.

3440 Control, Stop Printer: Causes the printer to become ready and inhibits printer interrupts.

3480 Control, Start Printer: Causes the adapter to gate 1132 emitter, and initiates a series of cycle steals which prints a single line of data.

3700/3701 Sense Device: Load status of device indicators into A. Indicators (t) are reset by 3701 command only.

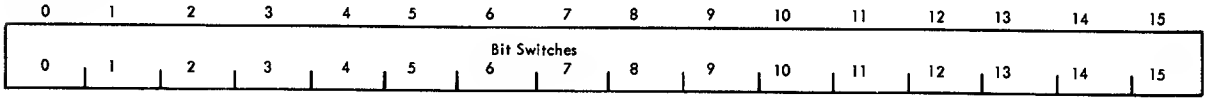
Device Status Word



Console Entry Switches, Interrupt Run Switch, and Program Stop Switch

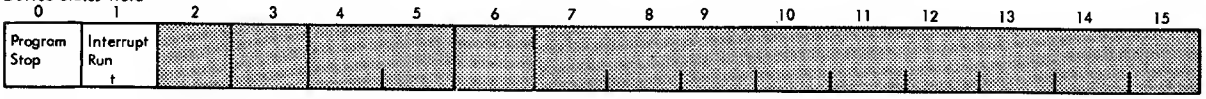
3A00 Read: Store contents of switches at C (IOCC address)

Data Word



3F00 Sense Device: Load status of indicators into A. Indicators are reset upon execution of this command.

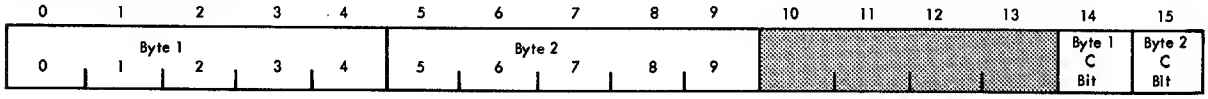
Device Status Word

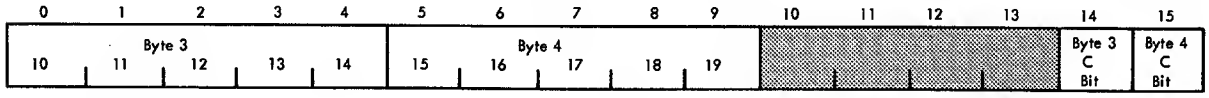


1231 Optical Mark Page Reader

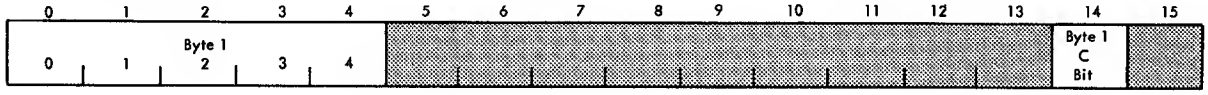
4200 Read: Store contents of output buffer, of the delay-line storage, at C(IOCC address).

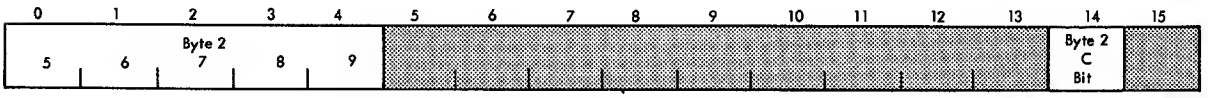
Data Words (2 Byte Transfer)





Data Words (Single Byte Transfer)





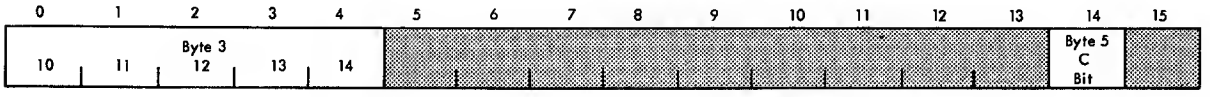


Figure 1-30. XIO Operations (Part 4)

1231 Optical Mark Page Reader - Continued

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
15	16	8yte 4 17	18	19										8yte 4 C 8it	

4402 Control, I/O Disconnect: Causes the reoder to stap the reoding of o page ond clears the delay-line storage of all dota.

4404 Control, Start Read: Causes o page to move through the read station and reads the dato into the delay-line storage.

4480 Control, Select Stacker: Causes the page just read to be placed in the alternote stacker.

4700/4701 Sense Device: Load status of indicatars into A. Indicatars (t) are reset by 4701 command.

Device Status Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Reod Response t	Tlming Mark Error t	Read Error t	Master Dato	Operation Complete Resp t	OK To Select	Feed 8usy	Document Sel by OMPR	Test Tim- ing Mark Chk Busy	Happer Empty				Reod 8usy	Busy	Not Ready

2501 Card Reader

4E00 Initiate Read: Causes the adopter to transfer the number of wards speclfied by the word count ta C (1OCC address) using the cycle steal mode. The 2501 data word is identical to 1442 dato word.

Program Load Reod: Identical to the 1442 program load read. The program load read data ward is identical to the 1442 program load dota ward.

4F00/4F01 Sense Device: Laad status af indicatars into A. Indicators (t) are reset by 4F01 cammond.

Device Status Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Error Check	Last Card	Operation Complete t										8usy	Not Reody or Busy

Synchronous Communications Adapter

5100 Write, Load 8uffer: Causes the 1131 ta transfer C (1OCC address) ta the SCA buffer.

Dota Ward

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
N	X	O	R	8	4	2	1								

5101 Write, Turn Off Audible Alarm: Causes the SCA audible alarm ta be turned aff.

5102 Write, Turn On Audible Alorm: Causes the SCA audible alarm ta be turned an.

5104 Write, Sync/Idle Chorocter: Causes the 1131 to transfer C(1OCC address) to the SCA sync/idle register. The narmal sync/idle character is shown belaw.

Sync/Idle Character

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	1	1	1	0	0	1								

5200 Read, Load Core from 8uffer: Couses the SCA ta transfer the cantents af the buffer to C (1OCC address).

5201 Read, Diagnostic Read 1: Causes the SCA ta transfer the condition af 9 triggers to C (1OCC address). The data ward is shown belaw.

Diagnostic Read 1

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Synch- ronize Trigger	Idle Character Trigger	Character Complete Trigger	End Operation Trigger	Diagnos- tic Mode Trigger	Binary Timer Trigger	3 sec Timer	1.5 sec Timer	Send Data / Space Bit							

Figure 1-30. XIO Operations (Part 5)

Synchronous Communications Adapter - Continued

5202 Read, Diagnostic Read 2: Similar to Diagnostic Read 1. The data word is shown below.

Diagnostic Read 2

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Clock Gate Trigger	Sync Counter Trigger	1st Transition Trigger	Phase Cntr Ctrl Trigger	Receive Tag Trigger	Character Phase Trigger	Optional Test Point for CE Use									

5401 Control, Set 7 Bit: Allows the SCA to transmit and receive data using a 7-bit character format.

5402 Control, Set 6 Bit: Allows the SCA to transmit and receive data using a 6-bit character format.

5404 Control, End Operation: Causes the SCA to be reset and disconnected from the line if jumpers are installed. This command also sets the SCA to the 8-bit character format.

5408 Control, Diagnostic Mode: Causes the SCA to establish and interrupt at each bit shift, allowing the CE to check the operation of the SCA.

5410 Control, Synchronize: Causes the SCA to establish synchronization with the remote terminal.

5420 Control, Start/Stop Timeout: Causes the timer trigger to be set (if turned off) or reset (if turned on).

5440 Control, Disable: Inhibits the SCA auto answer request interrupt circuit.

5480 Control, Enable: Causes the SCA to interrupt on receipt of an auto answer request.

5500 Initiate Write, Transmit: Sets the SCA in the transmit mode.

5540 Initiate Write, DC Reset: Causes the adapter triggers controls and registers to be reset.

5600 Initiate Read, Receive Mode: Sets the SCA in the receive mode.

5601 Initiate Read, Master Mode: Turns on the recieve run trigger which places the SCA in the master mode (used to transmit data records).

5602 Initiate Read, Slave Mode: Turns the receive run trigger off and places the SCA in the slave mode (used to receive data records).

5700/5701 Sense Device: Load status of indicators into A. Indicators (†) are reset on execution of the 5701 command.

Device Status Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Read Response †	Write Response †	Check	Time-out †	Answer Request †	Busy	Enabled	Ready	Receive Run							

1403 Printer

A900 Write: Causes the carriage to skip to the channel specified by the modifier bits in the data word specified by C (IOCC address).

Carriage Skip Data Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
				1	2	3	4	5	6	7	8	9	10	11	12

AC00 Control: Causes the carriage to space one line.

AD00 Initiate Write: Causes the adapter to transfer the number of words specified by the word count from C (IOCC address) to the print buffer. The data word is shown below.

Data Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	40	20	10	8	4	2	1		40	20	10	8	4	2	1

AF00/AF01 Sense Device: Load status of indicators into A. Indicators (†) are reset by AF01 command.

Device Status Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Parity Check	Transfer Complete Inter †	Print Complete Inter †	Carriage Interrupt †		Ring Check	Sync Check					Carriage Channel 9	Carriage Channel 12	Carriage Busy	Printer Busy	1403 Not Ready

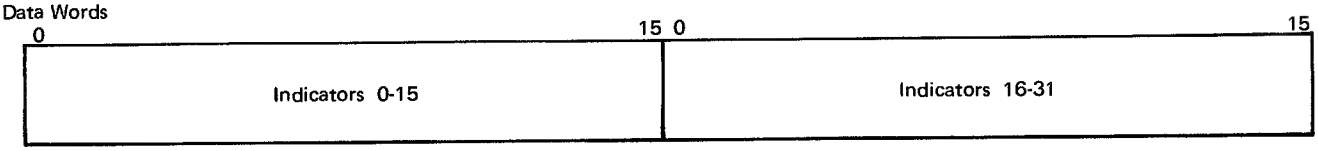
Figure 1-30. XIO Operations (Part 6)

2250 Display Unit

CD00 Initiate Write, Start Regeneration: Start Execution of display program. See 2250 Display Unit Reference Charts for format of control and display orders.

CD80 Initiate Write, Set Programmed Function Indicators: Loads programmed function keyboard indicators.

Data Words



CE00 Initiate Read: Reads 6 words into core storage.

Status Words 0-5

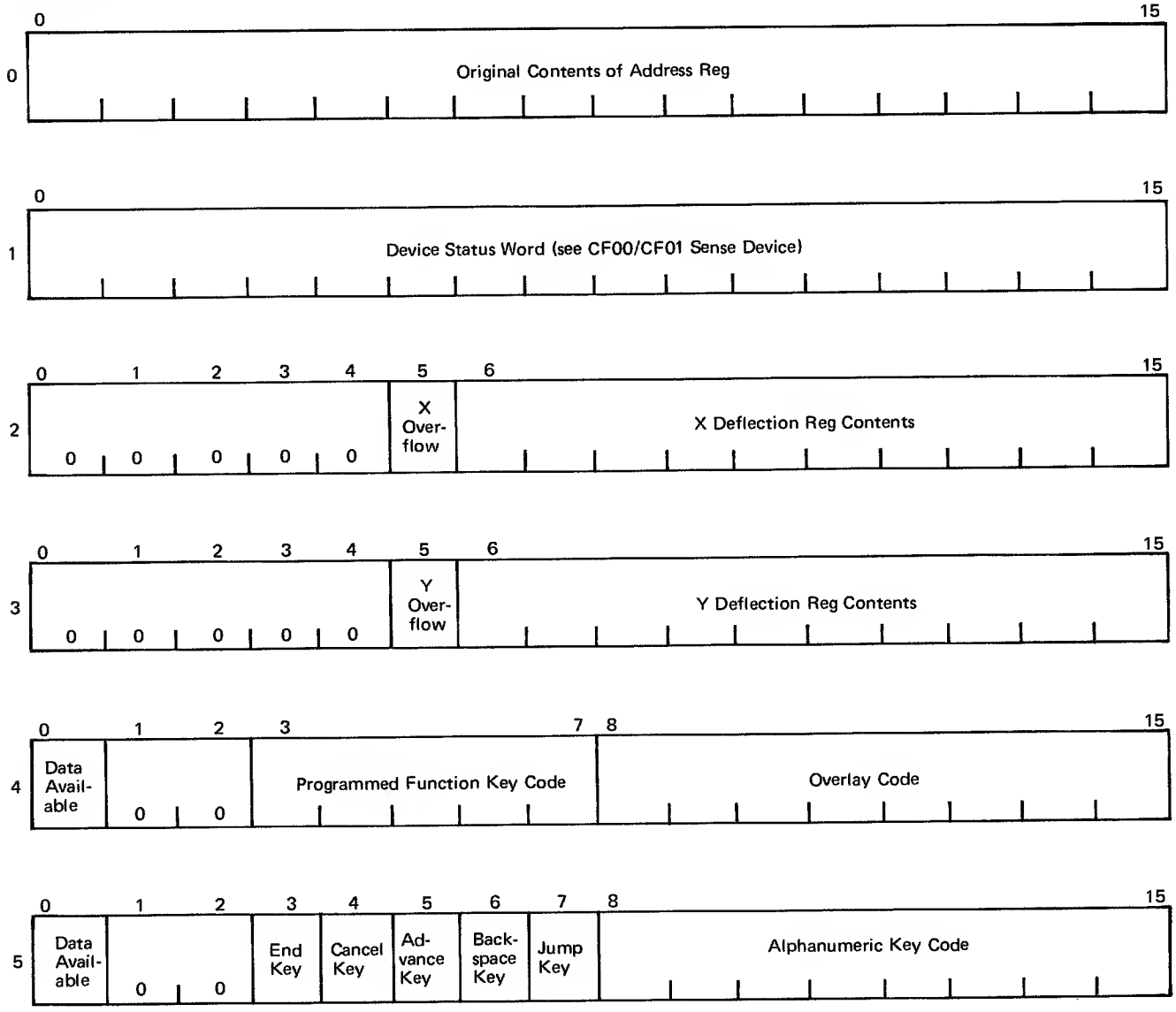


Figure 1-30. XIO Operations (Part 7)

2250 Display Unit - Continued

CE10 Initiate Read: Reads 14 status words into core storage
Status Words 0-5 (same as for CE00)

Status Words 6-13

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
6	Revert Register															

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
7	Programmed Function Indicators				Delta Counter					Stroke Reg			0	Stroke Reg		
	0	15	16	31	0	1	2	3	4	X-0	X-1	X-2		Y-0	Y-1	Y-2

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
8	—	Console Select	Inter-rupt Request	Sense ILSW	Diag-nostic Cmnd	Sense DSW	Data Req	Run S-Clock	0	Read Status	Gate Low	D-Reg Full	0	0	0	0

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
9	—	Mode Decode	Remem 2 Dis-place-ment	Enable Light Pen Irpt	Enable Light Pen Detect	0	0	—	Store Revert	Long Addr Word	Indi-rect Addr	Long Branch Com-plete	0	0	0	0

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
10	2-Word Abso-lute Data	Com-pute Delta	Gate Abs & Inhib X-Y	2-Word	Gate Incre-mental Data	Incre-mental Char Data	0	0	Remem Over-flow	0	Point Inten-sify	Line Inten-sify	0	0	0	0

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
11	Stroke Decode	Char Branch	Last Stroke	Large Size Char	Super-Script	Sub-script	Char Data Req	Revert	0	0	0	0	0	0	0	0

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
12	Write PF, Indi-cator	PF Key Zero **	0	A/N Key Actu-ated **	A/N Key-board Strobe **	Shift **	Alter-nate **	S-Clock > 3 *	S ÷ Clock							
									S-7 *	S-6	S-5	S-4	S-3	S-2	S-1	S-0

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
13	Pulse Stop Counter							Pulse Stop Cond	0	0	0	0	0	0	Force Analog Defl. Com-plete	Analog Defl Not Com-plete
	64	32	16	8	4	2	1									

* Reset to one.
** Inverted output.

Figure 1-30. XIO Operations (Part 8)

2250 Display Unit - Continued

CC00 Control, No-operation: Ignored by 2250.

CC80 Control, Reset Display: Stops regeneration and generates a unit reset.

CF00/CF01 Sense Device: Load status indicators into accumulator. Indicators (†) are reset by CF01 command.

Device Status Word

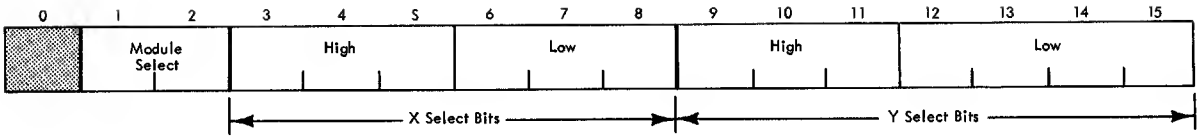
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Order Controlled Interrupt	Keyboard Interrupt	Detect Interrupt	Cycle Steal Check	Detect Status	0	0	Light Pen Switch	Busy	Character Mode	Point Mode	0	0	0	Address Displacement	

CF10 Sense Device: 2250 address register to accumulator.

CF08 Sense Device: 2250 revert register to accumulator.

CF04 Sense Device: 2250 temporary register to accumulator.

Figure 1-30. XIO Operations (Part 9)



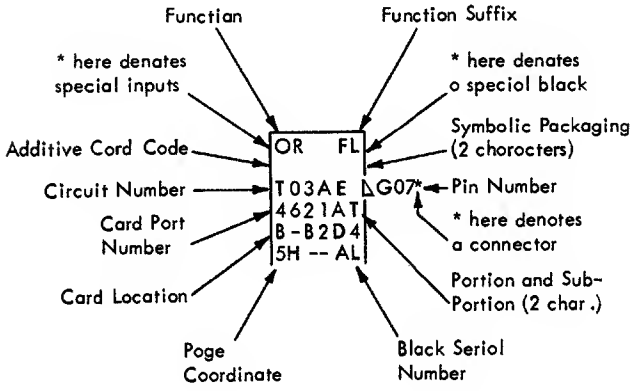
8K Module	Select Bits	
	1	2
1	0	0
2	0	1
3	1	0
4	1	1

Note: In troubleshooting core storage, it may be desired to substitute (or switch) storage modules. The module jumper wiring is shown on logic pages SA111 (2.2 μs) or SD331 (3.6 μs).

Figure 1-31. Storage Address Register Word Format

1.1 AUTOMATED LOGIC DIAGRAMS

1.1.1 Logic Block Symbology



1.1.2 Logic Page Identification

The logic page prefixes (major sections) used in the 1130 System Diagrams are shown in Figure 1-32. If a feature is not included in the machine type, no logics will be provided for that feature.

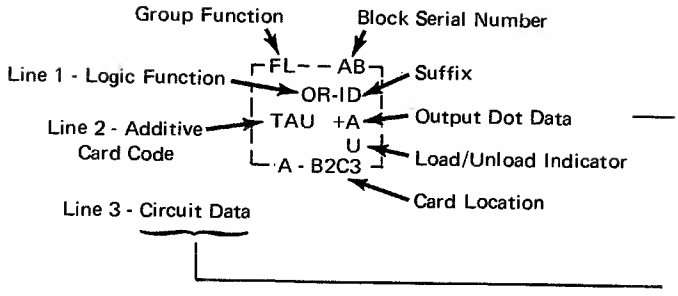
1.1.3 FE ALD Logic Block Information

Figure 1-33 provides general recall information for FE ALD logic blocks. For complete details and examples, refer to *Customer Engineering Memorandums* (General CEM Index # 1).

Major Section	Logic
AC	Socket Listing
AD	Additive Card Codes, Jumpers and Tie Downs, and SS Adjustments
AE	Signal Cable Terminations
AF	Solid Logic Design Automation Board Chart
BA	Socket Reservations and CE Card
BB	I/O Bus
BF	Socket Reservations
CR	2501 Card Reader Interface
DN	Operation Decode
DU	IOCC Decode
FA	Storage Access Channel I Adapter
FC	Binary Synchronous Communications Adapter
FD	1231 Optical Mark Page Reader Adapter
FR	2501 Card Reader Adapter
FX	1133 Multiplexer Control and Storage Access Channel II Adapter
GA through GD	2310 B Disk Storage Adapters (Drives 1 through 4)
GA and GE	2311 Disk Storage Adapters (GA = Drive 1, GE = Drive 2)
HP	1403 Printer Adapter
KA	CPU Oscillator
KB	CPU Branch Controls
KC	CPU T Clock
KD	CPU Instruction Cycle Timer
KG	CPU Register Controls
KM	CPU X Clock, Cycle Steal Controls, and Interrupt Controls
KR	Parity Check Controls
KU	Index Register Controls
KW	Usage Meter Controls
MB	Core Storage Address Bus
MC	Core Storage Read/Write Controls
RA	A and U Registers
RB	I, B, and M Registers
RD	D Register
RN	Format and Tag Registers
RQ	Q Register
RS	Cycle Control Counter
SA	2.2 μs Core Storage
SD	3.6 μs Core Storage
WF	Single Disk Storage and Core Storage Interfaces
WZ	Core Storage Interface
XC	Console
XF	Single Disk Storage Adapter
XG	1627 Plotter Adapter
XP	1132 Printer Adapter
XR	1442 Card Punch, or 1442 Card Read Punch Adapter
XT	Paper Tape Reader and Punch Adapter
XW	Console Keyboard/Printer Adapter
YG	1133 Power
YP	1131 Power
Z-	Reference

Figure 1-32. 1130 System Logic Prefixes

BASIC LOGIC BLOCK FORMAT



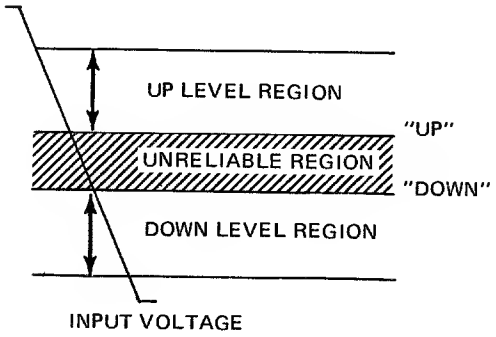
When the only input is an input to a dot block, the dot function and polarity are indicated; for example, +A or ◺ O.

The type of information appearing here depends on the circuit involved.

- Standard Circuit. This is a logic circuit that:
  1. Conforms exactly to its function and
  2. Requires input voltages that can be expressed by voltage code(s). For standard blocks, only the voltage code(s) is printed in the circuit data location.

Code	Up	Down	Code	Up	Down
B	+2.5	+1.5	P	unassigned	
C	+2.5	+1.0	Q	"	
D	+1.9	+1.0	R	"	
E	+2.0	+ .6	S	"	
F	+4.0	+ .3	T	+ .3	− .3
G	+2.5	+ .3	U	unassigned	
H	+2.0	+ .3	V	"	
J	+1.5	+ .3	W	"	
L	+ .6	+ .3	Y	"	
M	unassigned		Z	"	

Voltage codes and definitions are shown on the left.



The codes define Up and Down levels that, if met or exceeded, provide reliable operation of the circuit. The actual voltages normally observed will probably exceed these values. This is to be expected; the values stated are the minimum requirements under normal circumstances. For example, the "H" code denotes that the correct Up level is +2.0 volts or greater, and the correct Down level is +.3 volts or lower. These levels are often referred to as the threshold or transition values of a circuit.

Multiple voltage codes are printed if the logic block requires different levels on two or more input pins.

Figure 1-33. FE ALD Logic Block Information (Part 1)

1.2 SLT MAINTENANCE

Maintenance procedures for standard SLT components are found in the *IBM Field Engineering Theory of Operation (Manual of Instruction), Solid Logic Technology Packaging, Tools, Wire Change Procedure,* SY22-2800.

1.2.1 SLT Contact Wear

Avoid unnecessary removal and replacement of pluggable SLT components. The gold contact surfaces of SLT cards, cable cards, and board pins are rated for 50 insertions. Voltage crossover assemblies and other back-panel connector blocks are rated for 20 insertions.

1.2.2 Wire Color Codes

Panel wiring in the 1130 system conforms to the standard SLT color code designations: yellow identifies wiring that is controlled by computer-generated rework instructions, blue/white identifies uncontrolled wiring, blue identifies temporary wiring installed by REA (Request for Engineering Action), and black and yellow twisted pair is used for I/O cables and temporary flat cable repairs.

1.2.3 Machine Cable Folds

Figure 1-34 shows the most frequently used types of SLT flat cable folds in the 1130 system.

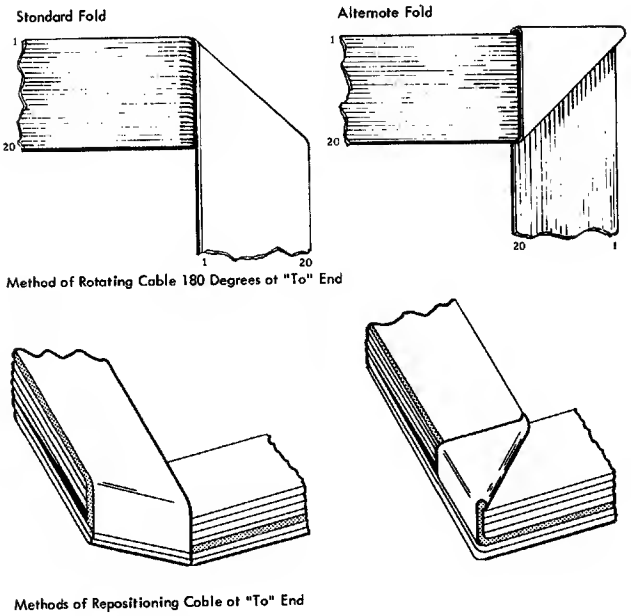
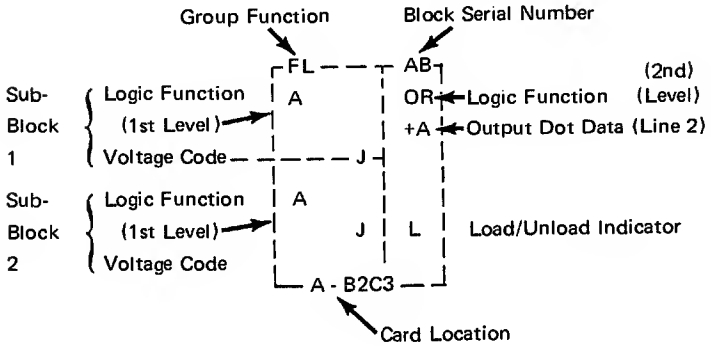


Figure 1-34. Machine Cable Folds

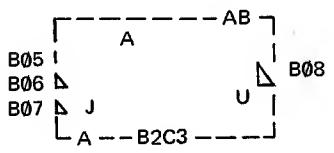
COMBINATIONAL LOGIC BLOCK FORMAT



Combinational Blocks

Multiple blocks are combined into "butted" or combinational blocks under the following conditions:

1. The blocks are all on the same card.
2. The inter-connections between the blocks do not connect to any other block, and no pins exist between the blocks.



Interpretation of Edge-of-Box Characters

Rule: Each input edge-of-box character indicates the level required on that pin to satisfy the function.

Each output edge-of-box character indicates the level of that pin when the function is satisfied.

Figure 1-33. FE ALD Logic Block Information (Part 2)

1.3 FAILURE LOGGING

Logging is the first procedural step to isolating and determining a system failure. One type of logging can be considered immediate: the error has occurred and continues presently to occur, with maintenance required (a failure); the second type, historical: the error has occurred, and may or may not be presently occurring or require maintenance.

1.3.1 Immediate Logging

Immediate logging is performed by error detectors. The CE may use diagnostic hardware and diagnostic maintenance program readouts.

1.3.2 Historical Logging

Historical logging for the 1130 system is of four types: (1) readouts of the customer's operational program, (2) the operator's log, (3) non-operational (error) readouts, and (4) CE Incident Reports.

1.3.2.1 Logging by the Customer's Operational Program

The records of all data processing inputs and outputs provide an indication of what was supposed to happen, versus what actually happened to the customer's process. These records provide clues as to where, when, and how the failure occurred or is occurring. The customer should keep and maintain an orderly library of such information.

1.3.2.2 The Operator's Log

The Operator's Log is a record manually written by the customer (operator, systems engineer, programmer, etc.) which is intended to state machine/process, human, and environmental conditions.

The log can contain valuable diagnostic information based on the operator's observations. Typically the operator's log will contain the time information is observed, the type of process being controlled, any change in the process inputs/outputs, and any change in environmental conditions concerning the process or the 1130 system. If an error or failure has occurred, all of the foregoing information should be included as well as the type of error or failure, when, where, and possible conjecture as to how the error or failure occurred.

1.3.2.3 Non-Operational (Error) Readouts

Programming checks in the form of non-operational or error readouts (pre, post, and during operations) may be provided for data processing input/output. Limited process I/O checks may also be provided at the customer's discretion.

1.3.2.4 CE Incident Report

Previous CE Incident Reports at the installation may serve as a clue to failure location and detection. These reports may be especially helpful in locating transient failures.

1.4 FAILURE DETECTION AND TROUBLESHOOTING

Detection can only take place through diagnostic hardware indicators (for transient and hard failures) or external service aids (for random failures). To assist in isolating a detected failure, manual controls and diagnostic programming have been included in the system's capability.

A failure can be physically located in (1) the 1130 system's programming, (2) the 1130 system's hardware, or (3) the customer's equipment other than the 1130 system. Repair and maintenance of customer's equipment is solely customer responsibility.

The service philosophy of the 1130 system is based on the effective use of diagnostic programs and techniques. These programs and techniques depend heavily on the multiple modes of operation of the processor and of the console indicators to define problem areas. It must be recognized that the programs and techniques cannot always eliminate the need for detailed pulse and voltage checking, but they are designed to reduce this detailed evaluation to a minimum.

When a failure occurs, note all pertinent information. Record the contents of all registers and console panel indicators on a check sheet for later reference. Try to localize the failure before removing the machine from productive work.

A failure in the +12 or +48 volt power supplies does not cycle power down in the 1130 system. If either the +12 or +48 volt supply has a power failure, the system will not operate and these power supplies should be checked first to determine that they are functioning.

The increased reliability of electronic components suggests that the majority of general service problems are electromechanical in nature. These problems are caused by mechanical adjustments, mechanical wear, electrical timing, and loose connections.

Diagnostic procedures have been provided to assist in isolating troubles between the electronics of the processor and the functions of electromechanical peripheral devices.

Keep in mind two other problem sources, program troubles and electrical noise troubles. Because the 1131 processor depends completely on programming for all input and output functions as well as for processing, program timing errors and incorrect data can appear as electronic processor or I/O problems. The diagnostic programs are designed to exercise and examine the functions of the processor and I/O devices. In general, the tests provide the assurance needed to guide problem analysis to the machine or the program. Electrical noise can be a problem because of the low level signals used in this and other solid state systems. Critical evaluation during tests assures that the system is free from electrical noise interference anticipated in most environments. Suppression circuits have been designed into the system to reduce exposure to both internal and external interference. However, there is always the possibility of unique external conditions or of the failure of grounding or suppression circuits. While there are no unique tests or tools available to pinpoint electrical noise, the diagnostic section of this manual does provide some analysis procedures which can assist trouble analysis when electrical interference is suspected.

Note: For problems that do not seem to lend themselves to analysis, check that all cards and interboard connectors are in place and seated.

1.4.1 Error Detection

All data entering core storage has odd parity added to each half word. The parity is checked when reading out of core storage. A parity error in core results in the processor stopping at the end of the core storage cycle in which the parity error condition is detected. Parity bypass is under CE switch control, not under program control.

These I/O devices provide error indicators in their corresponding Device Status Words (DSW): Disk Storage, 2310B Disk Storage, 1132 Printer, Communications Adapter, 1403 Printer, 2501 Card Reader, 1442-5,6,7 Card Read Punch, and the 1231 Optical Page Reader. In addition the printers, card readers, card punches, and the optical page reader have visual indicators on the device to alert the operator to the fact that an error has occurred. System diagnostic programs provide error handling techniques for program recognizable input data errors, and supply printouts to aid in diagnosing troubles.

1.4.2 Error Isolation

The CE switches under the right hand top cover provide specific functions for processor error isolation. Bit switch data can be written into core and then read back for parity verification. Bit switch data can be cycled through the processor and registers without reference to storage. Interrupt request can be inhibited. Indicator lamps can be mass tested.

In addition to the CE switches, four modes of operation (single step, single cycle, single instruction, and interrupt run) are available at the console. These modes are described in detail in 1.4.4.

To further assist error isolation, the single disk storage can be disconnected from the system and operated in the read mode under CE switch control. The processor can also be operated independently of the disk storage when it has been disconnected from the system.

The I/O devices are capable of limited mechanical operation independent of the processor. In general, independent mechanical operation of the devices cannot be performed without affecting processor performance.

It is possible to remove the devices from the system by disconnecting their signal connectors. In some cases it is necessary to ground interrupt level lines to permit operation of the processor with the device removed. If an I/O device is removed from the system for maintenance, use Logic AD000 to determine which lines must be grounded to maintain processor operation.

The console I/O printer cable connections are identical to those on a 1053 except for one wire and can be tied into the OLSA tester by interchanging the wire from H7 to R8 at H7 with the wire on H8. The 1053 jumper card (part 747579) is needed to attach the female plug on the I/O printer cable to the female connector in the OLSA. The console printer must be returned to normal before the system is returned to the customer.

If an I/O device is removed from the system, the program must not address that unit or the program may hang up waiting for a device interrupt.

If it is desired to bypass the error stop when a 1442 read error occurs, isolate pin D05 of the card in location A-B1H2 (ALD XR291). If it is desired to bypass a punch error, isolate pin B05 of the same card. This allows operation of the 1442 in spite of the error condition. Be sure the circuit is restored to normal before returning the system to the customer.

1.4.3 Dynamic Detection

Within the processor, all data is parity checked when being read from core storage. A parity error results in an immediate stop of the processor if the parity run switch is off. Parity errors can be bypassed for CE analysis.

The most basic dynamic detection tools are the system diagnostic programs. Function, unit, and timing tests provide error handling capabilities and error looping routines to facilitate problem analysis. Within the diagnostic programs, unit device failures are handled with device status word bits. The sensing of these bits under program control results in printouts or halts which can be analyzed to identify the unit and type of failure and guide corrective action.

Intermittent error logging is a useful tool. Such logging can provide data to evaluate system integrity. It can also assist off line analysis and reduce system downtime to a minimum. Logging facilities can be designed into customer programs but are presently not available as a part of the system programming packages.

1.4.4 Static Detection (CE Control)

The following modes of operation are under switch control to assist the CE in analyzing and detecting machine failures.

Run Mode: The system functions as a normal processor. Program detectable errors under diagnostic test operation result in halts, printout routines, punchout routines, or a combination of these. Diagnostic tests provide for looping within specific functional areas under console entry switch control during the main diagnostic program. Diagnostic tests are built from basics and increase in complexity, providing a high degree of serviceability.

Run Interrupt Mode: A level 5 interrupt occurs after each mainline instruction. This mode can be used for tracing mainline, branch, or subroutine operations.

Single Instruction Mode: The processor stops after each instruction is executed. The start key controls the advance.

Single Machine Cycle: The processor executes a single clock cycle (T0-T7, E, I, IX, IA, etc.) under control of the start key. SMC can be used to investigate CPU functions with every cycle taken by memory.

Single Step: The processor executes a single clock step, i.e., T1 under control of the start key. Pressing the single step key results in the generation of an A pulse; releasing the key results in a B pulse.

Exercise care when using single step because core data can be destroyed if the processor is reset or if the mode switch is changed between T0 and T6 time.

1.4.5 Special Techniques

Failure to Program Load (Card System): (Figure 1-35). The initial problem is to define whether the card reader or the processor is at fault. The following procedure can assist diagnosis:

1. Try one-card programs. If these programs do not lead to an immediate fault location, load core with hex 7000 (MDX), using the bit switches and the storage load switch. Press reset and start the program by pressing the start key. This causes the processor to perform a no-op operation. By changing the displacement through core, the instruction operates as a branch. If the MDX instruction operates properly, enter hex C000 (load accumulator) in location 0000. Enter hex D000 (store accumulator) in location 0001. Reset the CPU and press the start key. This simple routine loops and sets hex D000 in every core location. If these routines run, check the system using Figure 1-35.
2. An incorrectly adjusted 1442 read emitter causes intermittent loss of interrupts. In this case the last words in the read in area are blank and the data read is in adjacent positions. Failure to read a column (assuming an interrupt occurs) results in blank words within the 80-word field causing a read register check or a feed check. Double incrementing of the I counter on program load causes blank words in core on program load.

Card Feeding (No Program): A technique for causing the 1442/2501 to feed cards without a program in the machine is sometimes needed. This technique is:

1. Load the read hopper with cards.
2. Turn the mode switch to single step (SS).
3. Press the program load key.

1442: Cards continue to feed as long as the program load key is held. The program load key may be blocked down and the feeding controlled by the 1442 start and stop keys.

2501: Cards continue to feed without holding the program load key. Reset key must be pressed to stop feeding cards.

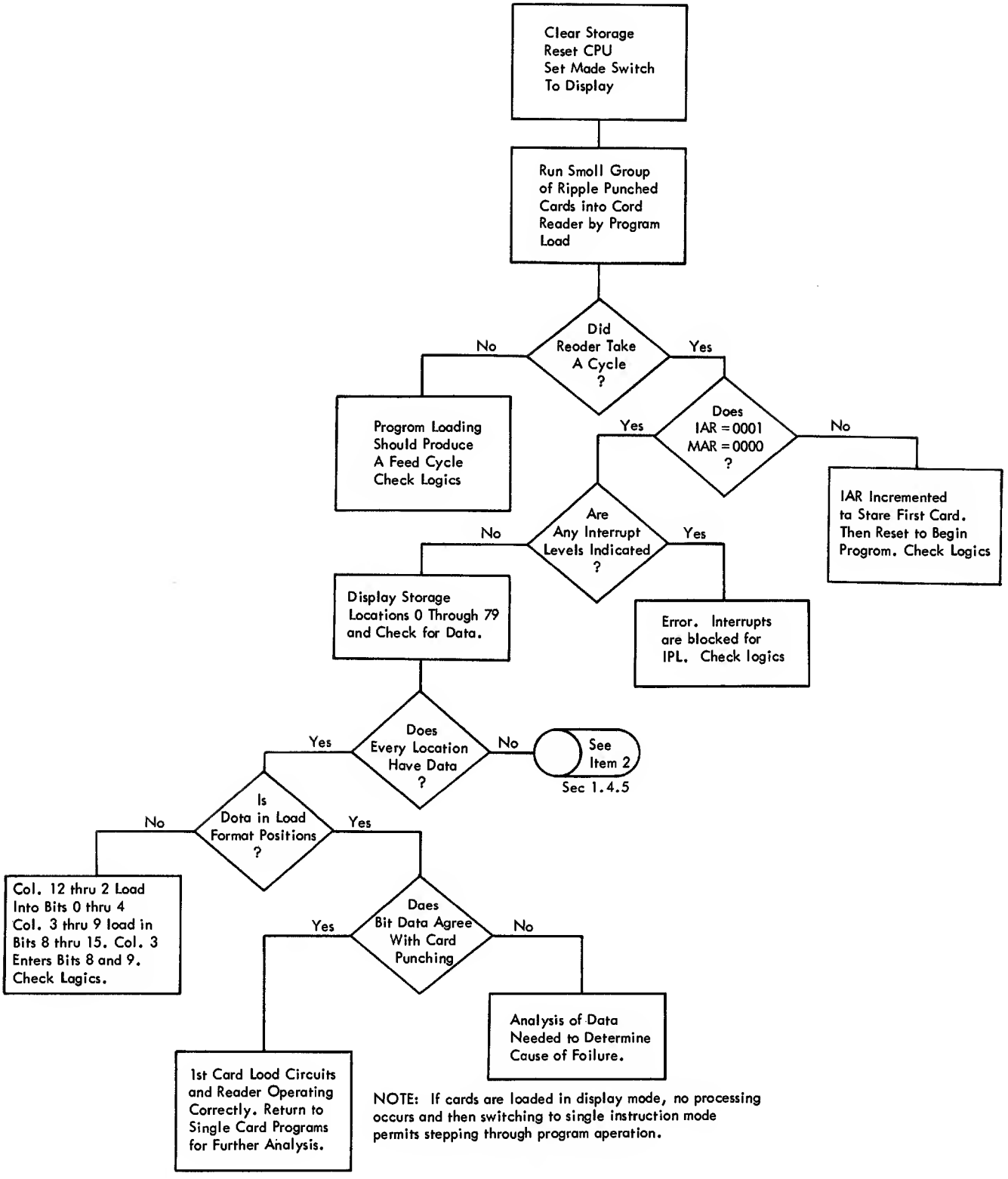


Figure 1-35. 1442 Program Load: Flow Chart

1.5 THE MAINTENANCE DIAGRAM MANUAL (MDM)

The following paragraphs define the organization and contents of this manual.

1.5.1 IBM 1130 Configurator

This diagram defines the maximum system configuration.

1.5.2 System Data Flow Diagram

This diagram shows the overall data flow of the 1130 and the exits and entries to the I/O devices.

1.5.3 Unit Data and Control Diagram (UDCD)

This diagram expands each unit contained within the system data flow diagram to include major controls.

1.5.4 I/O Operations Diagrams

These diagrams show the overall functions of I/O operations in positive logic diagrams.

1.5.5 Simplified Logic Diagrams (SLDs)

These diagrams consist of simplified (second level) logic diagrams of the complex areas of the system where an additional level of logic is desired for clarity.

1.5.6 Logic Flow Charts (CLFC)

The diagrams show, in condensed form, the concept of a particular operation.

1.5.7 Timing Charts (T)

These diagrams depict the timing conditions of applicable operations.

1.6 DIAGNOSTIC PROGRAMMING AND MACHINE CHECKOUT

Diagnostic programs provide rapid diagnosis of many system troubles. The console panel is useful for controlling manually entered tests used when diagnostic programs cannot be run.

1.6.1 Maintenance Diagnostic Programs

The information on the diagnostic programs presented here is for general use only. Detailed descriptions of the programs and their use are provided with the programs. The maintenance programming system was developed to test and check, as completely as possible, the data paths, checking circuits, control functions, timing relationships, registers, mechanical adjustments, and I/O interaction. The various programs that test the individual machine functions permit detection, provide degrees of localization, and communicate to the CE those indications of machine status which assist him in repairing the problem rapidly.

1.6.2 Program Language

The maintenance program system is programmed using the 1800/1130 standard assembler program language. The listings follow the standard assembler program format and include comments and explanations to help the CE understand and follow the program operation.

1.6.3 Program Control

Manual control of the maintenance program system is provided as follows:

1. Stop or continue on error.
2. Loop program, loop routine, loop function, or loop on error.
3. Bypass or allow error typeout.
4. Bypass or allow manual intervention requests.

1.6.4 Error Messages and Documentation

These items are included in either the error messages or documentation, or both.

1. The location in the program of the failing routine or function.
2. The cause of the program halt or error message.
3. The function or functions that failed.
4. A comparison of the actual results with the expected results.

1.6.5 Program Loading

The maintenance programs are provided on cards and paper tape.

1.6.6 Tests for Device Interaction

The diagnostic monitor has the facility for controlling up to six test programs simultaneously, depending on core size, to provide overlapped or interacting operation of devices.

1.6.7 Operation Modes

The maintenance programs are designed to run in one of two modes, independent mode or dependent mode.

1.6.7.1 Independent Processor Tests

These programs assume complete control of the system and run independently of any other program. All I/O functions and interrupt controls are handled within the program. Errors are indicated by error halts which are described in the documentation.

Function Tests: These tests are engineered specifically to exercise and evaluate each of the functions of the system.

The function tests are designed to provide thorough fault detection (data-, sequence-, and interaction-related problems may not necessarily be detected by a function test), with short run time and minimal program size.

These programs use the building block approach; that is, the simplest instruction is tested first and no instruction is used to test another instruction until it has been fully tested itself. The procedures for running the tests are given in the CPU test index in the test documentation.

Tests included in the independent mode are:

1. CPU function test.
2. Core storage function test.
3. Core storage adjustment test.
4. Basic diagnostic loader.
5. One-card diagnostic programs (7).
6. Interrupt test.
7. Data-path tests (see one-card-programs description).

The data-path tests are used when none of the other function tests will load. To diagnose this type of trouble, the CE must use the test facilities provided on the console. Instructions are entered one at a time through the bit switches, and the instruction operation can be evaluated by the CE.

1.6.7.2 Monitor Controlled I/O Tests

These programs run under control of the diagnostic monitor and may be overlapped. Errors are indicated by error messages printed out on the 1131 Console Printer.

All I/O programs run under control of this monitor. Under this control, programs can be run one at a time, run in a predetermined sequence, or run simultaneously in any combination, except as limited by core size.

Two versions are available, card and paper tape. Program selection is via the bit switches.

This program controls the I/O function tests and incorporates the functions of housekeeping, program loading and execution, interrupt handling, error handling, and Customer Engineer communication, such as printouts. The documentation provides an I/O monitor test index to aid in running these tests.

The following programs are provided:

1. Paper Tape Reader/Punch function test.
2. 1131 Console/Keyboard function test.
3. 1132 function test.
4. 1442 function test.
5. 1442 timing test.
6. 1627 function test.
7. Disk storage function test.
8. Disk initialization program

1.6.7.3 1130 Maintenance Diagnostics Part Numbers

The part numbers of the diagnostic programs and of the program documentation are given in Figure 1-36.

Program	Program Listing	Card Deck Or Paper Tape	Documentation	1131 Model 1, 2, and 3 Volume	1131 Model 4 Volume
1. Monitor	2191200	2191201	2191202	3	3
2. CPU Function Test	2191204	2191205	2191206	1	1
3. Core Storage Function Hi	2243964	2243965	2243966	2	1
4. Core Storage Function Low	2243967	2243968	2243966	2	1
5. Disk Storage Function Test (Basic and 2310)	2191212	2191213	2191214	3	
6. Disk Initialization Program (Basic and 2310)	2191216	2191217	2191218	3	3
7. 1132 Model 1 Function Test	2191220	2191221	2191222	4	
8. 1442 Function Test	2191224	2191225	2191226	4	3
9. 1442 Timing Test	2191228	2191229	2191230	4	3
10. Paper Tape Function Test	2191232	2191233	2191234	4	
11. 1627 Function Test	2191236	2191237	2191238	4	1
12. Console/Keyboard Printer Function Test	2191240	2191241	2191242	4	2
13. Core Adjustment Test	2191244	2191245	2191246	2	2
14. Meter Test	2191248	2191249	2191250	2	
15. Basic Diagnostic Loader	2191252	2191253	2191254	1	1
16. One Card Diagnostic Programs	2191260	2191261	2191262	1	1
17. Interrupt Function Test	2191268	2191269	2191270	2	2
18. SAC	None				
19. SCA Instruction Function Test	2243565	2243566	2243567	5	
20. SCA Write/Read Buffer and Line Noise Detection Test	2243572	2243573	2243574	5	
21. SCA Wrap Around Test	2243568	2243569	2243570	5	
22. SCA Transmit/Receive - STR	2191278	2191279	2191280	5	
23. 1442 Relocating Loader	2191281	2191282	2191283	3	2
24. 2501/1442 M5 Function Test (Test Cards 2243549)	2243550	2243551	2243552	4	
25. 1403 Printer Function Test	2243556	2243557	2243558	3	
26. 1231 Optical Reader Function Test	2243553	2243554	2243555	3	
27. SAC II	None				
28. Paper Tape Relocating Loader	2191286	2191287	2191288	3	
29. 2501 Basic Loader	2243559	2243560	2243561	1	
30. 2501 Relocating Loader	2191284	2191285	****	3	
31. SCA Display Program	2243562	2243563	2243564	5	
32. CE Utility Programs	2243957	2243958 (Note 2)	(Note 1)	2	
33. Scope Loops	2243962	2243963	—	2	2
34. DIMAL	2243959	2243960	2243961	2	2
35. SCA Transmit/Receive - 8SC Point to Point	2243971	2243972	2243973	5	
36. SCA Transmit/Receive - BSC Multi Point	2243974	2243975	2243976	5	
37. SCA Transmit/Receive - 8SC 8K point to point	2243977	2243978	2243979	5	
38. Meter	5889431	5889432	5889433		2
39. Disc Storage Function Test	5889425	5889426	5889427		3
40. 1132 Model 2 Function Test	5889422	5889423	5889424		3
41. Disk Storage Function Test (2311)	2483293	2483291	2483292		
42. Disk Initielization Program (2311)	2483290	2483288	2483289		

Note 1 Disk Adjustment Prog 2243957
Scope Loops 2243962
} Documentation & Listing

Note 2 Disk Adjustment & Scope Loops are provided by this part number.

**** Use Relocating Loader PID 03AA-03A8-03AC

Figure 1-36. Maintenance Diagnostic Programs

1.7 SERVICE CHECK LIST

1.7.1 General Information

1. On what operation does the machine fail?
   a. Diagnostic test.
   b. Customer work (FORTRAN, etc.).
   c. Op code during which failure occurred.
2. What is the frequency of error?
   a. Time of day.
   b. Environment (temperature, etc.).
   c. Does customer power fluctuate at certain time of day (welder, heavy machinery, etc.)?

1.7.2 General Check List

1. Have connectors and cards been checked for looseness or for bent contacts?
   a. Edge connectors.
   b. Laminar bus (pins and terminals).
   c. TB connectors (power supply, power sequence, etc.).
2. Have grounds been checked? (See 1.12.1)
   a. DC isolated ground.
   b. AC isolated ground.
   c. Ground straps (check contact from the gate to the frame).
3. Have power supplies been checked?
   a. Voltage levels
   b. Ripple.
4. Have fans and blowers been checked?
   a. Power supply fans.
   b. Gate fans and blowers.
5. Does the machine fail on margins? Normal margins are ±4%.

1.7.3 Core Storage Check List

1. Which lights are on?
2. Has indicator lamp test switch been checked?
3. What is the pattern of the failure?
   a. Greater or less than 4k; odd or even, etc.?
   b. Picking or dropping bits?
   c. What bits are affected?
4. Is the trouble in B register rather than core storage?
5. Core storage air flow correct?
6. Has component substitution been tried?
7. Have the sense lines been scoped?

CAUTION

Use an insulated probe tip when scoping core as shorts in the core area can damage the core array. When adjusting pots in the core circuits, use the plastic alignment screwdriver, part 460811, to avoid shorting to other cards.

Adjustments of the core storage timings and voltages should not be changed until proven to be out of tolerance. Always use the Tektronix 453 oscilloscope and Weston 901 meter or their equivalents when checking and/or adjusting core storage timing or power supply circuits.

1.7.3.1 Solid Core Failure, Limited Area of Failure

1. Record mode of failure.
   a. Bit pickup or dropout.
   b. Addressing failure.
2. Record pattern of failure.
   a. Build table of failures.
   b. If Y drive line is open, replace cards.
   c. If X drive line is open, replace cards.
   d. Make continuity check for open drive or sense lines (paragraph 1.7.3.4).
   e. Check diodes on array (paragraph 1.7.3.4).
   f. Remove array; check welds and wires visually.
   g. If core is bad, replace array.

1.7.3.2 Solid Core Failure, General Failure (All Addresses or All Bits)

1. Turn on the storage load CE switch.
2. Turn on all bit switches.
3. System cycles through all of core and tries to enter all bits.
4. Check SLT voltages to core (+6, +3, -3).
5. Check +12v and output of regulator voltage at 8.5v.
   a. Adjust voltages if out.
   b. Replace regulator card.

   Note: Do not replace the regulator card if the output is ground, as the new card will be shorted out.

6. Check timing signals: read/write, long time/short time, strobe, emitter strobe.
7. Check V reference and VSA voltages.
8. Check X and Y current by scoping voltage test points.

1.7.3.3 Core Failure, Intermittent

1. Check SLT voltages to core (+6, +3, -3).
2. Check +12v and output of regulator voltage at 8.5v.
3. Check timing signals.
4. Check V reference and VSA voltages.
5. Check X and Y current by scoping voltage test points.

1.7.3.4 Core Parity Errors

The basic approach to correct interpretation of core parity problems, particularly intermittent troubles, is to record both data and address information and then analyze the data for failure pattern. Address decoding is based on a 3,3,3,4 (bits 3 thru 15) bit grouping rather than on a straight hex grouping, so address errors need to be converted from hex to this grouping to determine address sensitivity. See ALD SD021.

Shorts or opens in the array unit have been a significant part of the intermittent parity problem. The failures can frequently be aggravated with concentrated heat (hair dryer) directed on the array or with vibration including slight deformation of array by twisting on array handles.

Raising the temperature of the core storage board by blocking the air flow may also result in an increase of failure rate.

Shorted or open diodes and shorts between pins at the edge of the array boards should be field analyzable and repairable. Opens have also occurred at the edge of the array boards. These may not be readily obvious to the eye as the epoxy may be holding the connection mechanically. Use ALD SD011 through SD082 and ohmmeter to isolate.

Shorted diodes show as low output at all address groups except the one that has the failing diode. Maladjustment of core voltages and strobe may temporarily compensate for a shorted diode, but core will be operating at a marginal level and be highly susceptible to temperature or voltage variations.

Differential scoping of the sense lines will show low envelopes inside the outside envelope as shown in the following illustration

The low envelope will be a heavy trace indicating the groups with good diodes; the outside "normal amplitude" envelope will be a light trace of the group with the failing diode.

There is another shorting condition which occurs internally in the bottom board and is not field repairable. This is a leakage path between drive and sense lines. The failures usually start out very intermittently and increase gradually. Core storage adjustment and card swapping occasionally help but do not correct the problem.

There are three combinations of bottom board leakage. Each exhibits specific symptoms and can be identified with fairly simple measurement techniques. However, diode or array-point connection shorts and opens can exhibit similar symptoms.

Leakage Between a Drive Line (Or Group of Drive Lines) and a Sense Line.

Symptom: Bit pickup in a particular sense line for the addresses associated with the drive line.

Analysis:
1. Evaluate parity error data and addresses.
2. Remove jumper block associated with the failing bit position. (This last step isolates the array for further checking.)
3. Check for resistance between the sense line of the failing bit and all driver gate pins. See Logics SD021. This should essentially be an open circuit. A unit with 100k ohms of resistance will work, but experience has shown that units with a leakage path lower than several megohms will continue to deteriorate and eventually cause intermittent parity errors. Defective units have also exhibited a momentary breakdown from 5,000k ohms to 5k ohms under heat, vibration, or extended operation.

Solution: Replace storage unit.

Leakage Between Two Drive Line Groups.

Symptom: Dropping of any bits associated with the two groups. May also cause picking of bits, depending on magnitude of leakage.

High Resistance: Picked bits due to coupling noise to **sense line.**

Low Resistance: Dropped bits due to drain of drive current.

Analysis:
1. Evaluate parity error data and addresses.
2. Differentially scope the sense line output of any failing bit while regenerating an all 1s pattern. The 1s envelope will contain groups of low amplitude core outputs because of current splitting between the shorted drive lines.

Solution: Replace storage unit.

Leakage Between Two Sense Lines.

Symptom: Picking or dropping of bits on the two sense lines independent of addresses.

Analysis:
1. Evaluate parity error data and addresses.
2. Remove the jumper block(s) associated with the failing bits.
3. Check for resistance between the failing sense bit lines. See *Leakage Between a Drive Line and a Sense Line* for comments on resistance.

Solution: Replace storage unit.

Because of the mechanical construction and failure mechanism in the bottom board, most shorts due to bottom board failure have been between bits 0, 14, or 16 and one of the low order Y drive lines.

1.7.4 Addressing Failure Check List

Addressing failures can be very elusive because of the branching, indirect addressing, and effective addressing features of the CPU.

This list will help the CE isolate such failures:

1. Record all console indications of the failure (IAR, M register, and B register).
2. If cycle steal addressing trouble is suspected, it may be necessary to statically check the addressing circuits. The CE indicators can be wired to help evaluate the **addressing circuits.**
3. Using the core service techniques, try to evaluate whether the trouble is in core storage or in the addressing circuits.
4. Trace routines using the interrupt run mode of operation should be considered.

A simple routine which stores the IAR and returns to the mainline program on any branch or instruction is helpful to see how far the program progressed before it failed.

Be aware that this kind of operation can be misleading if the first branch is to data which is acted upon as an instruction.

1.7.5 Core Storage Console Isolation

1. Load system to all bits.
   a. Turn on the storage load CE switch.
   b. Turn on all bit switches.
   c. Turn the mode switch to LOAD.
   d. Press the start key.
2. Stop and reset the system.
3. Turn off storage load CE switch.
4. Turn on storage display CE switch.
5. Turn function switch to DISPLAY.
6. Press the start key.
7. Machine stops with a parity error.
8. Storage address register bits on indicate the failing X-Hi-or-Low, Y-Hi-or-Low driver (see Figure 1-37).

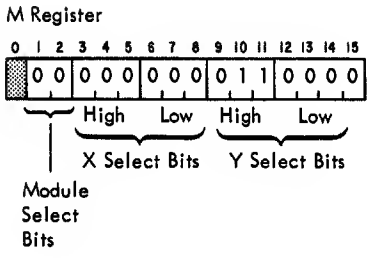


Figure 1-37. Example of Hi-or-Low Driver

The bad driver is Y-Hi-RD/write gate 011 at B-C1 G3 according to the core unit plugging chart, SD021.

If B register does not contain all bits, the trouble is in a sense/inhibit card. Picking bits may be checked by changing step 1b to: No bit switches on.

In the event of an intermittent failure, a recording of each failure must be made, indicating **the M register address and** B register contents and parity bits.

An M register bit on pattern should develop if the failure is in X or Y line circuits.

If no M register pattern is evident, examine the words in B register for a pattern. Remember that parity bits indicate which half of the word is wrong. A failure indicates a failing sense amplifier or an inhibit driver (same card).

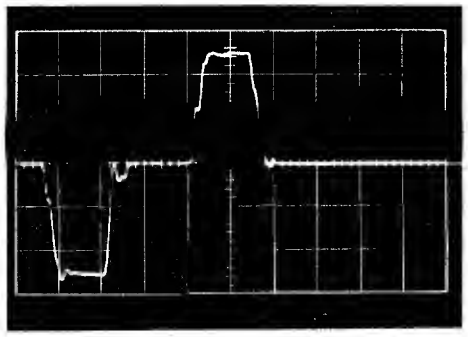
No pattern in either area indicates a problem in address or strobe time generation.

1.7.6 Current Scoping of Core

1.7.6.1 Initial Oscilloscope Setup

1. If a particular address is in question, load MDX *-1 (hex 70FF) into that address, using CE and bit switches, to provide a one instruction loop.
2. Oscilloscope: use Tektronix 453 or equivalent.
   a. Current probe in channel 1.
   b. Time base: 0.5 microseconds/div.
   c. Vertical input channel 1: 0.1v/div.
   d. Sync on rise of T0: +DC, external.
3. Core setup.
   a. Remove jumper block for position desired, using removal tool (part 2108860) and pulling straight out.
   b. Install ten 4" jumpers in place of the jumper block following the printed circuit pattern on the back of the block.
   c. Hang current probe on specific jumper.

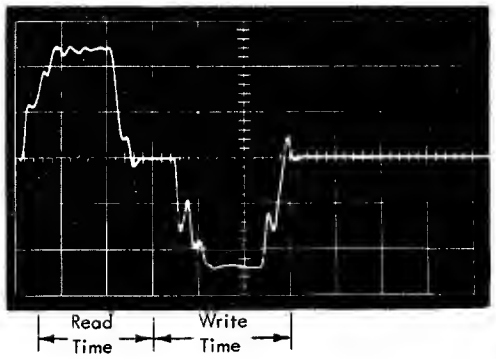
Y-Line Current



Oscilloscope setup:

1. Initial setup.
2. Channel 1: Y read gate, write driver B-C1K5B04.
3. Block at C1K5 removed and jumpered.
4. Reference SD221.

X-Line Current



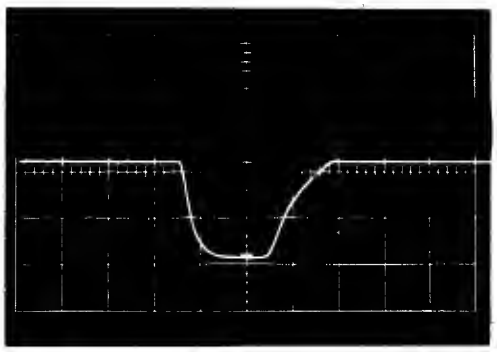
1.7.6.2 Core Array Waveforms

The following examples of core storage waveforms were obtained using a 453 oscilloscope plus the oscilloscope and core setup described in the section above, and hex address 0000.

Oscilloscope setup:

1. Initial setup.
2. Channel 1: X read gate, write driver B-C1J6B02.
3. Block at C1J6 removed and jumpered.
4. Reference SD222.

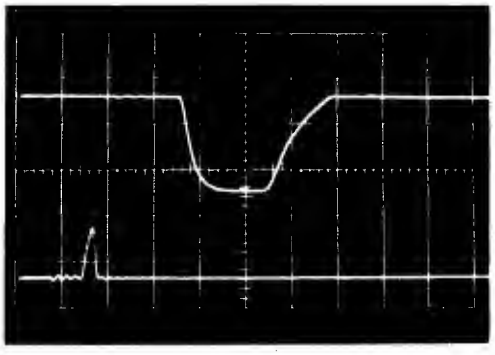
Inhibit Drive Current



Oscilloscope setup:

1. Initial setup.
2. Channel 1: inhibit bit 4 (bit 4 = 0) B-C1E7D04.
3. Block C1E7 removed and jumpered.
4. Reference SD403.

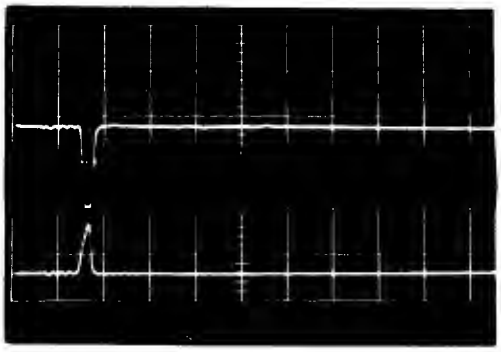
Sense Line With No Bit



Oscilloscope setup:

1. Initial setup.
   a. Channel 2 voltage probe.
   b. Channel 2 set to 0.2v/div.
   c. Mode switch set to ALT.
2. Channel 1: inhibit/sense bit 4 (bit 4 = 0) B-C1E7D04.
3. Channel 2: strobe pulse B-C1B6B07.
4. Block C1E7 removed and jumpered.
5. Reference SD403.

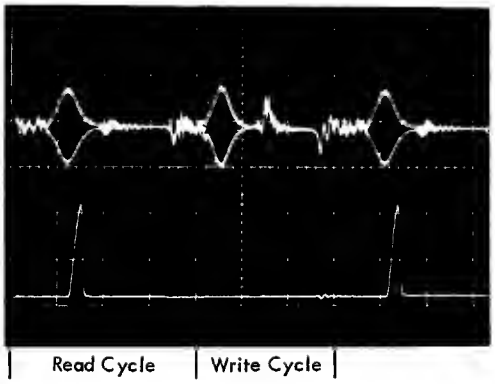
Sense Amplifier with a 1-Bit



Oscilloscope setup:

1. Initial setup.
   a. Channel 1.
      1. Voltage probe.
      2. 0.05v/div.
   b. Channel 2.
      1. Voltage probe.
      2. 0.2v/div.
2. Channel 1: sense amplifier 1-bit (bit 9 = 1) B-C1B3B10 (SD403).
3. Channel 2: strobe B-C1H2B09.

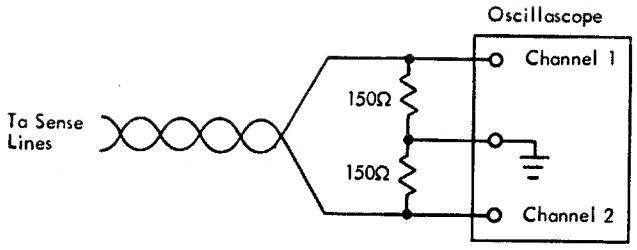
Inhibit Sense Lines – Bit 3 + 1



4k Machines Only

Setup:

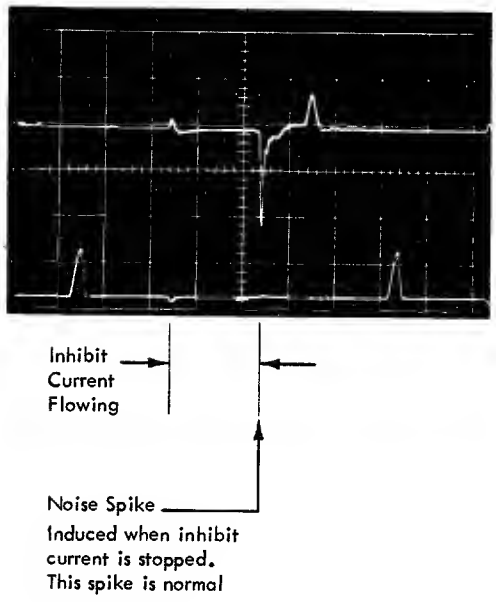
1. Console setup.
   a. Storage load and cycle switch on.
   b. Bit switch 3 on.
2. Oscilloscope setup.
   a. Channel 1 and 2 set on AC INPUT and 0.05v/cm.
   b. Invert channel 2.
   c. Vertical mode switch set to ADDED.
   d. Input to channels 1 and 2 are twisted pair wires set up as shown (part 2182907).



e. Sweep set to 0.5 microseconds/div.
f. Sync + DC external on T0 B-A1J2B13.
g. Connect twisted pair to B-C1B5B02 and B-C1B5D02 (SD403).

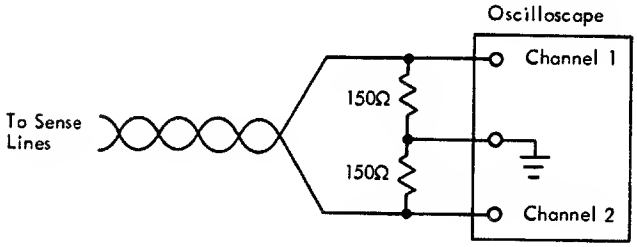
The first two envelopes are read cycle and write cycle, respectively. The lower trace is strobe; it is shown for reference only and cannot be obtained without special equipment.

Inhibit Sense Lines – Bit 3 = 0.



Setup:

1. Console setup.
   a. Turn on the storage load and cycle switch.
   b. Turn on bit switch 3.
2. Oscilloscope setup.
   a. Channel 1 and 2 set on AC input and 0.5v/cm.
   b. Invert channel 2.
   c. Vertical mode switch set to ADDED.
   d. Input to channels 1 and 2 are twisted pair wires set up as shown (part 2182907).



e. Sweep set to 0.5 microseconds/div.
f. Sync + DC external on TO B-A1J2B13.
g. Connect twisted pair to B-C1B5B02 and B-C1B5D02 (SD403).

1.7.7 Core Diagnostic Aids (Figure 1-38)

1. Core waveforms are the same while cycling core with either the CE storage load or display switch on. With the storage load switch on, parity errors do not stop the machine. Core is read out to the B register and read back in from the bit switches. With the display switch on and the parity run switch off, parity errors stop the machine. Core is read out to the B register and is read in from B register. Any bits dropped in this mode are lost. For analyzing a failure from the console, the display mode is probably best.
2. Current control card failures cause errors at random core addresses. Some addresses fail more often, but this is only because of circuit characteristics. To check the current control cards, turn on the CE storage load switch. Turn on the bit switches to the desired configuration and press the start key to CYCLE CORE. Scope B2B09 to check for Y dimension. X dimension (M2B09) duration corresponds to long time; Y dimension is short time. The amplitude of X and Y are equal and approximately 2v to 2.5v. This amplitude is a function of the V-Ref voltage. V-Ref can be checked against the voltage reading recorded on the core voltage label to see if it is correct.
3. Scoping the current control card test point (M2B09 for X, B2B09 for Y) shows if all read/write drivers are conducting. If a driver fails to conduct, there is a light trace across the bottom of the pulse for that dimension. If two drivers are conducting at the same time, however, these test points look normal.

   Two drivers conducting together split the current for that dimension, resulting in neither address reading or writing correctly. When the defective driver is addressed, it works correctly because no other driver is conducting. When a good driver is addressed, the defective driver conducts also, causing both to fail. If this failure is suspected, stop the increment of the I register (IAR) (jumper B A1M2G13 to D08) and cycle core in a failing address. Using a current probe, scope the X and Y dimension drive line for that address. (See current scoping technique, item 4.)

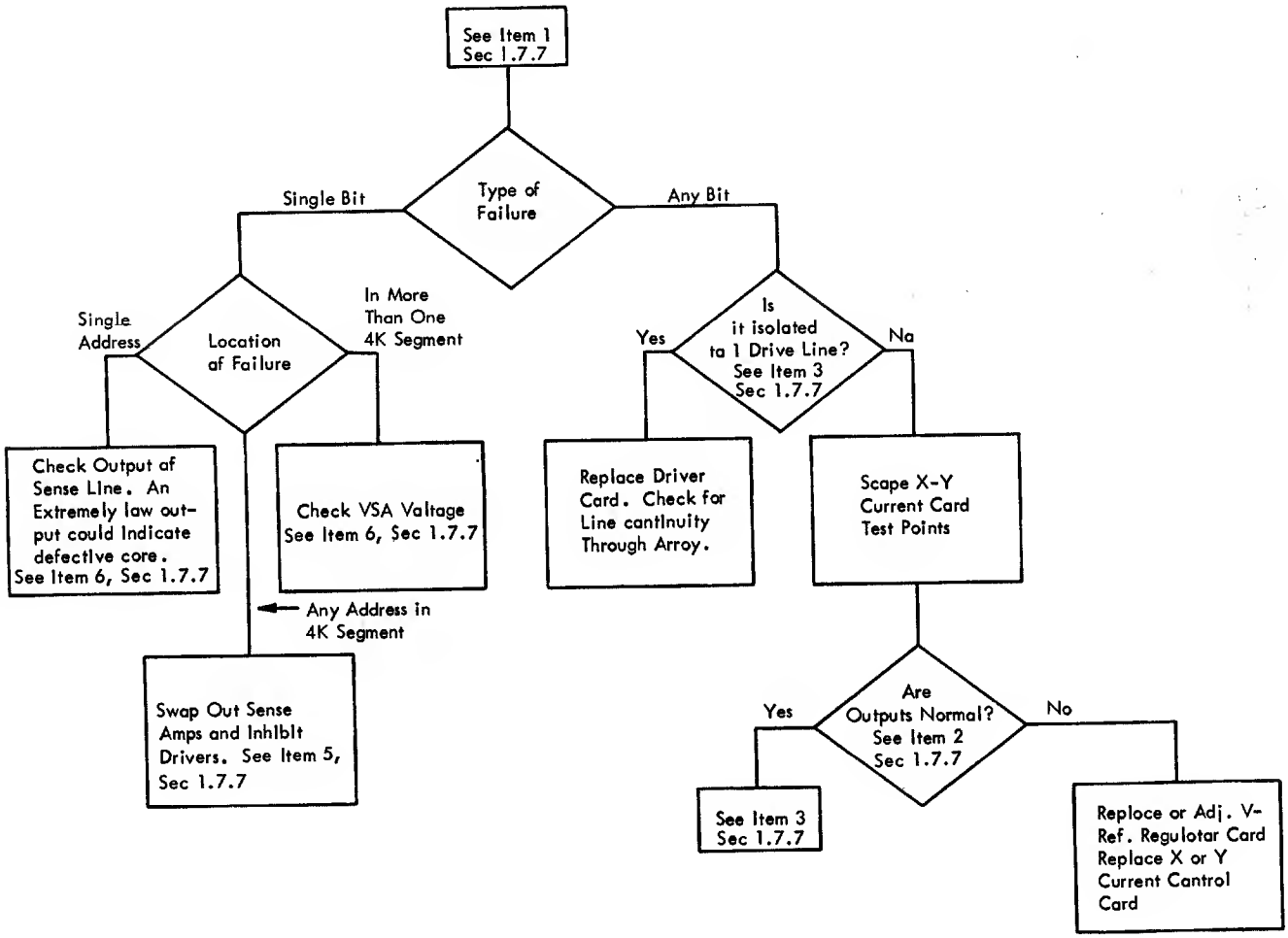


Figure 1-38. Core Flow Chart

There should be 210 to 265 ma through the lines. If one dimension has only half enough current, the failing driver is in that dimension. Analyze the failing addresses to find the defective driver.

4. Current loops are required in order to scope current on the 1131 core storage. The current loop block is put onto the pin side of the large board in place of the array connector block for the desired lines. Make up a current loop block using a single card extender, or offset, and the four-inch SLT jumpers. Install the jumpers to the same configuration as the array connector block jumpers (SD021).
5. There is one inhibit driver for each bit in each 4k of storage. If an inhibit driver never conducts, that bit enters 4k of storage continuously. If it always conducts, the bit can never be entered into that 4k. Any other 4k segment of core functions correctly. If there is a bit failure through 4k of core, exchange the inhibit driver and sense amplifier cards for that bit with another bit. If the trouble is not a card, but a sense/inhibit failure is suspected, check the continuity of the sense/inhibit line.
6. There is one sense amplifier for each bit in each 4k of core. The variable sense amplifier (VSA) voltage controls sensitivity of the sense amplifiers. The factory setting is recorded on the core voltage label. Scope the output of the sense line to the sense amplifier using a differential amplifier as shown in section 1.7.6.2. With the strobe single shot properly adjusted, the strobe output should coincide with the sense line output.

Figures 1-39 and 1-40 show diagnostic procedures for SJ-2 and SJ-4 core storage units.

1.7.8 Transient Power Line Noise

Power line noise is characterized by lack of pattern. If transient noise is suspected, alert the physical planning representative to the situation. Some symptoms that have been noted in the field are:

1. Highly intermittent failures.
2. Failure defies any analysis by pattern.
3. Failures occur mostly during the day (commonly related to the start or end of a work day when large numbers of equipment are being turned on or off).
4. Weekend performance relatively trouble free.

1.7.8.1 Methods of Determining Noise

1. Scope with the oscilloscope grounded on the power supply common.
   a. Suspected line.
   b. Ground pins on failing SLT boards (noise levels should be less than 1 volt peak to peak).
   c. AC input lines of contactors.
2. Indicator – A latch or line level can be wired into a CE indicator. The line may need to be gated to indicate only the transient pulse.

   Note: Bursts of transient line noise of up to 20v peak to peak normally do not affect the 1130 system if the noise is reflected by all power supplies in the system.

1.7.8.2 Methods of Aggravating Noise Problems

1. Determine what other equipment is on the 1130 line. Run a program while turning on and off the power switches on this equipment, i.e., air conditioning, units, heaters, other DP equipment, etc. (Check with customer first.)
2. Separate the ac and dc grounds from machine frame.

1.7.8.3 Areas to Investigate

If noise problems are encountered or suspected, check for the following:

1. Is system on a separate circuit?
2. Does system have a good ground return to power source (a separate ground circuit for the 1130 system)?

1.8 CONSOLE PANEL

The console bit switches and associated circuitry provide the ability to store in or read out from core storage data and programs. A complete description of the console panel and its uses are in Chapter 2.

1.9 CE PANEL

The CE panel has switches to aid the CE in his diagnostic procedures. Details on their use are given in Chapter 2.

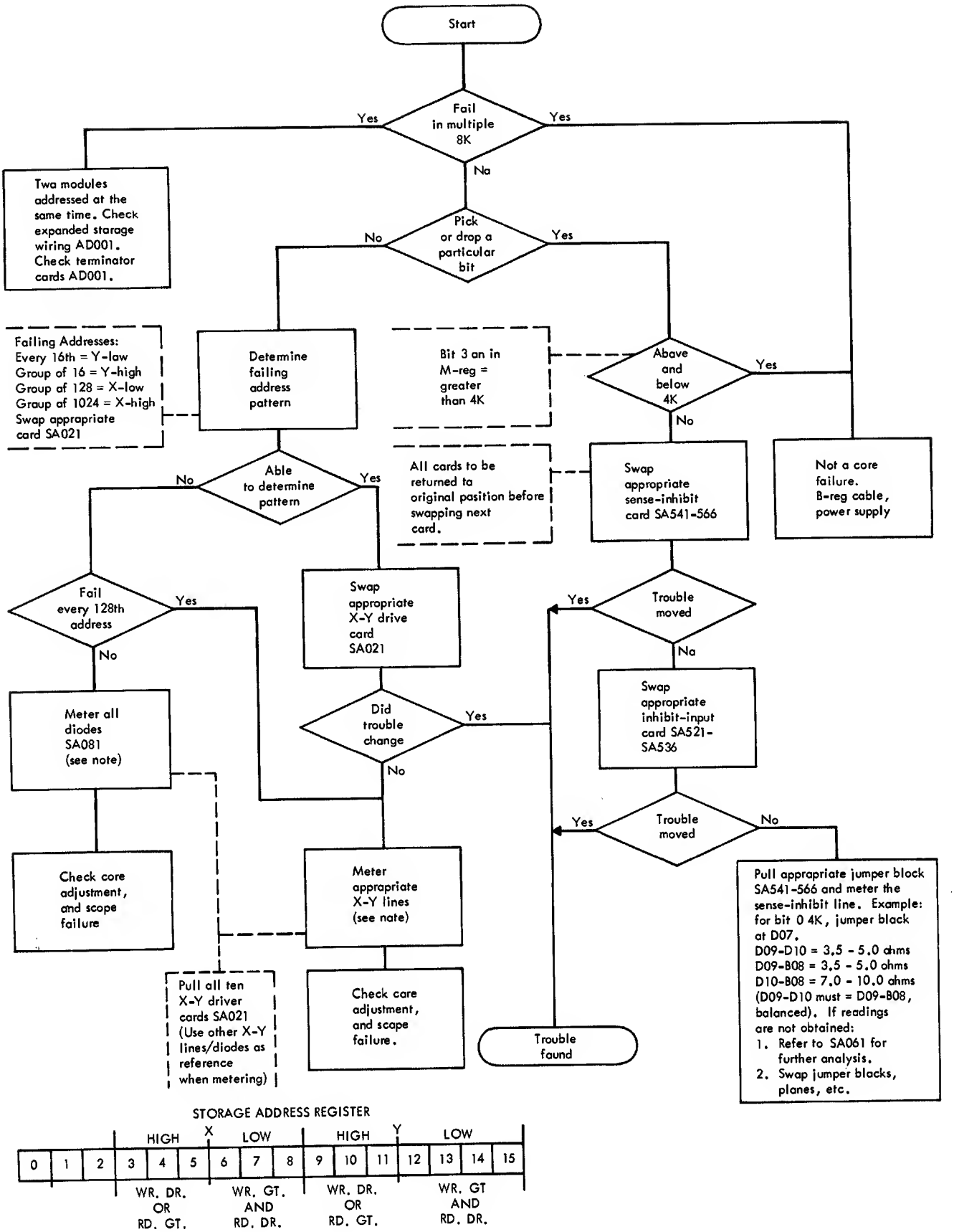


Figure 1-39. Core Storage Diagnostic Procedure (SJ-2)

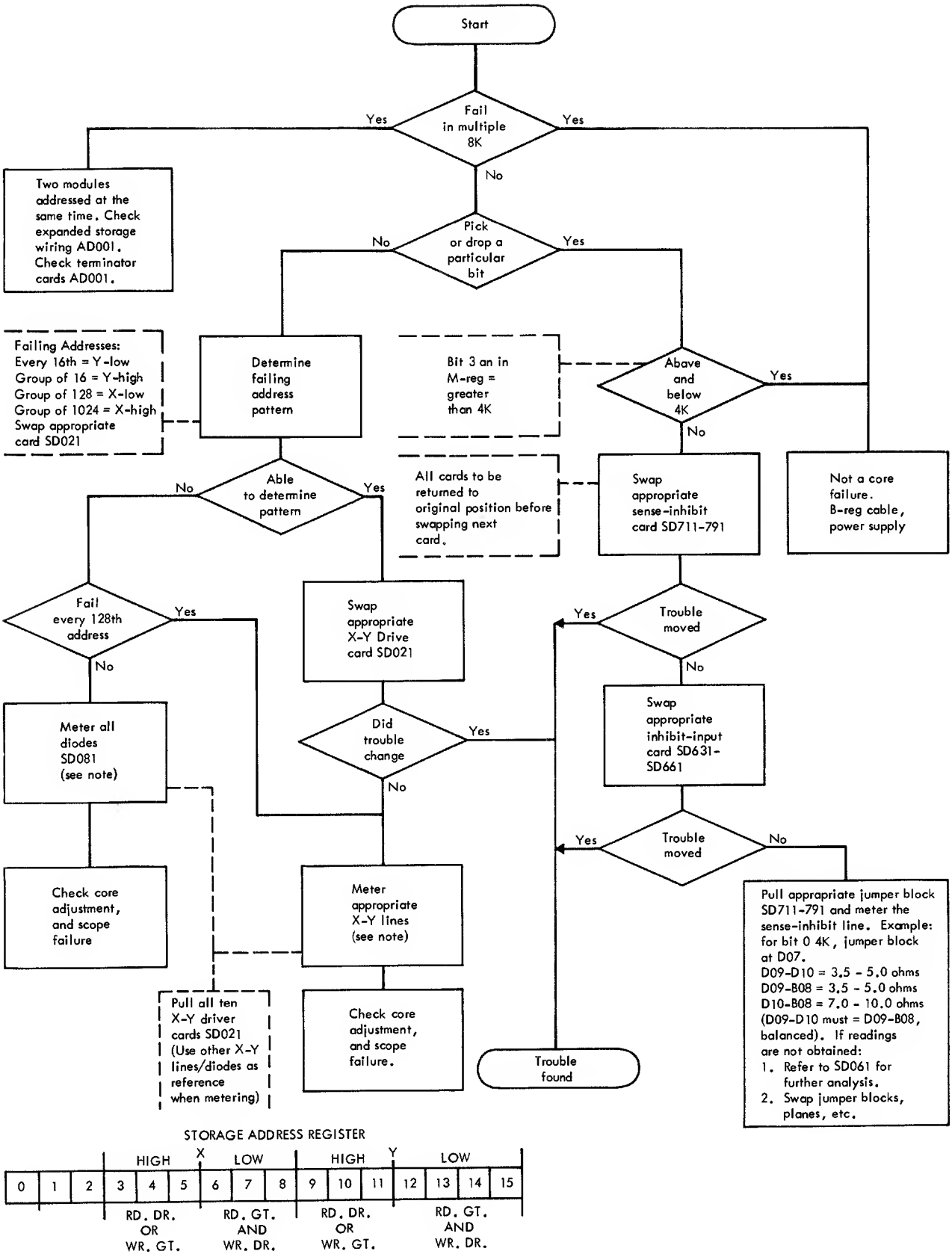


Figure 1-40. Core Storage Diagnostic Procedure (SJ-4)

1.10 CONSOLE PRINTER

1.10.1 Console Printer Diagnostic Aids (Figure 1-41)

1. Determine which data or control functions are failing. To determine which data functions of tilt or rotate are failing, check which characters are failing and use Figure 1-42 as a reference.

Example: Tilt 2 and tilt 3 characters do not fail.
Tilt 3 characters print for tilt 1 characters.
Tilt 2 characters print for tilt 0 characters.
These conditions indicate the function of T2 is at fault.

2. If there are failures in both data functions and control functions, determine if there is any relation between the failures, using Figure 1-43 as a reference.

Example: The data function T2 and control function of carrier return are failing. These two functions are related in that they both use character word bit 0.

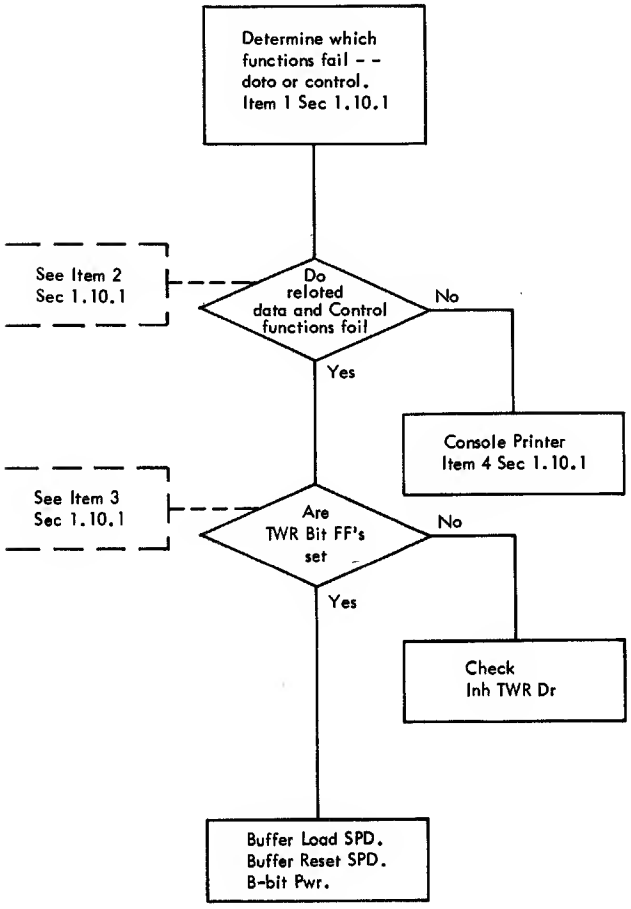


Figure 1-41. Console Printer Flow Chart

3. If there is a relation between data functions and control functions, check the associated 'TWR bit' FF to determine if it is being turned on. If it is being turned on, the 'INH TWR DR' line should be checked. If it is not being turned on, check the TWR buffer load SPD, TWR SPD, and the associated 'B-bit PWR' line.
4. Investigate the console printer if one of the following is true:
   a. Data functions fail and control functions do not.
   b. Control functions fail and data functions do not.
   c. There is no relation between data function and control function failures.

1.11 MARGINAL CHECKING

There is no marginal check supply on the 1130 system. However, the logic supplies (+3v and +6v) may be varied by ±4% and the system should still operate trouble free. Consider power supply variation only after other isolation techniques have been exhausted.

Voltage settings on the 1130 system are critical. A precision meter is required to set voltages. Always use the Weston 901 (or equivalent) meter when marginal checking or adjusting voltages.

Note: If it is necessary to power down the system while running margins, always return the logic voltages to the normal voltage. Logic supplies set to the high limits (+4%) can trip the regulator circuit breaker during the power-on sequence.

1.12 MISCELLANEOUS TECHNIQUES

1.12.1 Locating Grounds

1. Disconnect the following wires from TB4 (ac ground bus):
   TB4-13 (SCR ground).
   TB4-15 (ac to dc jumper ground).
   TB4-16 (ac to dc jumper ground).
2. Check for a resistance of no less than 10 megohms between:
   a. Each dc bus and the machine frame.
   b. Machine frame and the disk-storage base plate.
3. Locate grounds by disconnecting wires at the gates.

Note: With frame grounds removed on an isolated bus system, the electrical resistance between any two points (for example, ground pins on different transistor panels) should be 2.0 ohms or less.

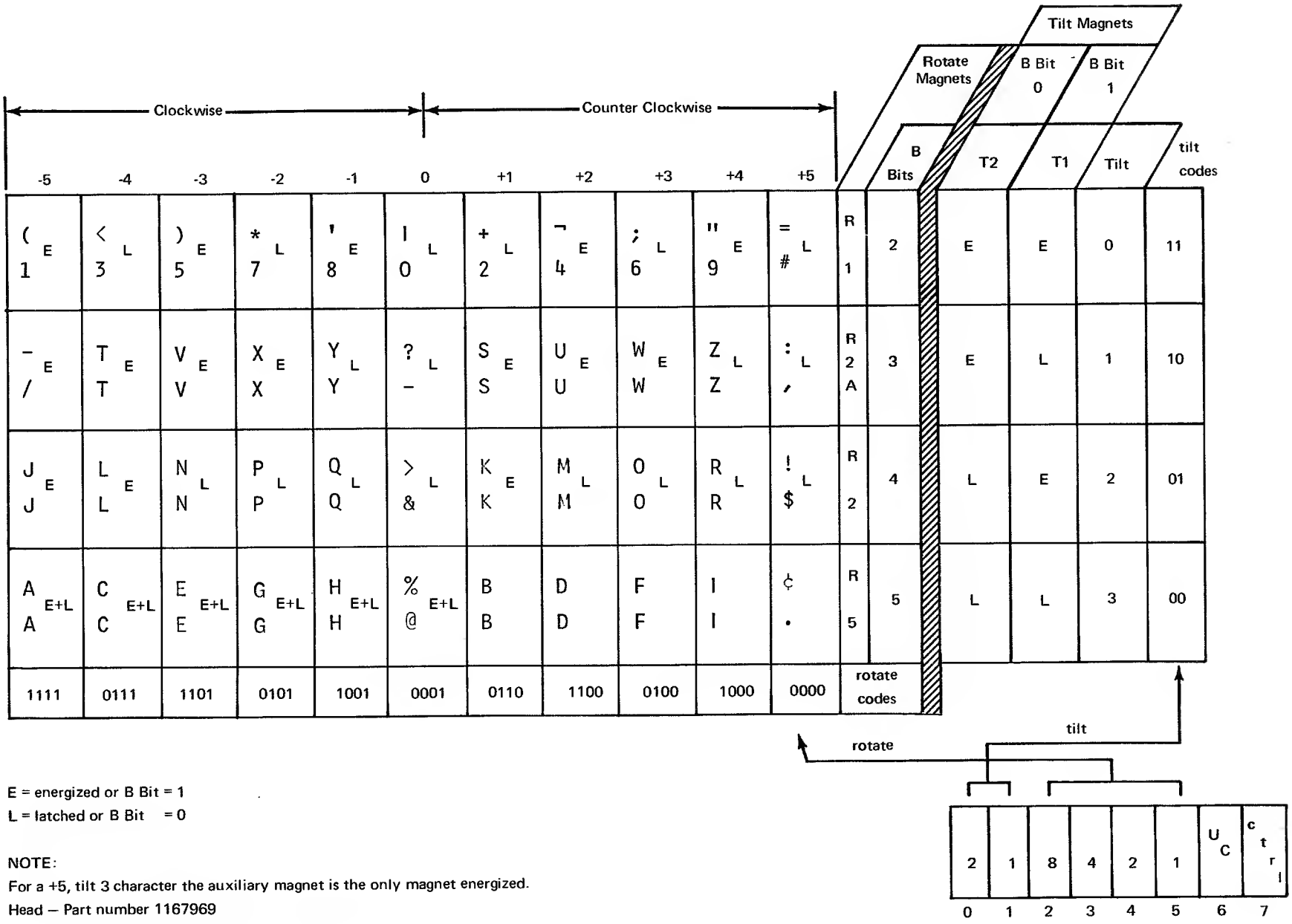


Figure 1-42. Typehead Chart

E = energized or B Bit = 1

L = latched or B Bit = 0

NOTE:

For a +5, tilt 3 character the auxiliary magnet is the only magnet energized.

Head – Part number 1167969

Last three numbers of part number on the head.

Character Word Bit	Data Function	Control Function
0	T2	Carrier Return
1	T1	Tabulate
2	R1	Space
3	R2A	Backspace
4	R2	Shift to Red
5	R5	Shift to Black
6	Upper Case	Line Feed
7	Used for Control Function	

Figure 1-43. Console Printer Word Chart

1.12.2 Locating Marginal SLT Cards

If an error shows when running the machine under marginal conditions, the SLT card giving the trouble can be found by isolating the gate where the problem is located by analysis of the circuit failing, e.g., I/O control, printer, CPU.

Note: When a gate that appears to be giving trouble is located, the CE may find that the actual marginal card is the card which is driving the card located in the gate indicated by the test. The marginal driving card can be in another gate.

1.12.3 Signal Levels

Acceptable signal levels are:

0v	Range +0.0v to	0.3v
+3v	Range +2.88v to	3.12v
Inverter inputs	Loaded upper level	0.9v

These values are to be used only as a guide. They are expressed in general terms only and are not true for all circuits. However, circuits operating outside of these ranges should be suspect.

If interchanging a card does not affect a level which appears to be marginal, consider the driving and driven circuits connected to the card.

Special voltages have been noted in the line titles.

1.12.4 Transistor Delay Times

The transistors in the 1130 have an inherent delay time; that is, it requires time to saturate the transistor and time to unsaturate the transistor. In general, it takes longer to unsaturate than to saturate a transistor. These delay times are known as turn-on delay and turn-off delay. They are a function of the type of logic block being considered and the rising or falling of the input.

The total delay in a series of logic blocks is the sum of the individual transistor delays. If too long a delay is experienced in a series of logic blocks, the individual logic blocks should be scoped to see which block has too long a delay.

SLT cards have transistors internally connected to form a series of logic blocks. Because these circuits are all mounted on one card and connected internally, there may be no external check points between logic blocks. (No input or output pins are shown in the systems diagrams.)

Note: Turn-off delays (unsaturating) are generally the longest.

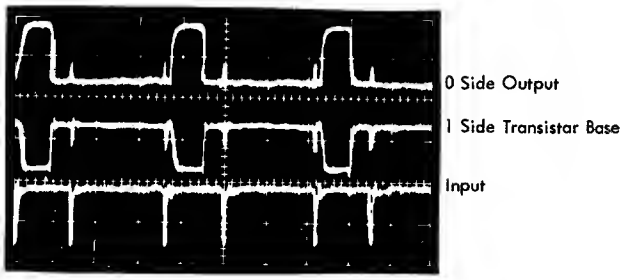
1.12.4.1 Measuring Transistor Delay Time

Transistor delays (slow or fast response) can cause intermittent machine failures that are difficult to diagnose. Circuit delays in the 1130 system are normally 15 to 30 nanoseconds. A slow circuit may cause delays on either the rise or the fall of a pulse and can be particularly troublesome in the 2.2 microsecond core storage. A method for measuring transistor delay follows:

1. Sync oscilloscope on the input to the card in question (while clock is running).
2. Probe the input and note the rise and fall time of the pulse.
3. Probe the output and compare with input pulse. The difference between the rise and fall times is the turn-on delay, and turn-off delay, respectively.

1.12.5 Multi-Input Flip-Flops

Spikes are sometimes observed in the output lines of multi-input FFs. When multi-input FFs are in one state and inputs are given to drive the FF into the same state, a spike is reflected in the off-side output.



These spikes are normal and the circuit design has taken them into consideration.

1.12.6 1442 Error Bypass

Read or punch errors from the 1442 can be bypassed by removing the 3794 card (location AB1H4) from the 1131 attachment circuitry. Removing this card disables the 1442 read and punch error sensing and does not affect other error sensing in the device.

This card must be replaced in location AB1H4 prior to returning the system to the customer.

1.12.7 2501 Error Bypass

Read errors from the 2501 can be bypassed by placing a jumper in the 1131 as follows:

AA1F6B04 to D08 (ground).

Section 3. Symptom Index

The Symptom Index is published by Plant Technical Operations (Boca Raton). The index is revised periodically and distributed to the field. File the current Symptom Index(es) for the 1130 system after this page and use it to locate all Service Aid CEM's and Engineering Change Announcements (ECA's) that pertain to the specified symptoms.

Section 4. Service Aids

Service Aids are published by Plant Technical Operations to keep customer engineers posted on troubleshooting techniques and service information. The Service Aids are distributed to the field in Customer Engineers Memorandums. File all Service Aids for the 1130 system after this page and use them to assist in trouble diagnosis.

Section 1. Basic Machine

2.1 MANUAL CONTROLS AND INDICATORS

The manual controls provide for manual operations during program and system analysis. The indicators provide a visual indication of machine and program status under the various modes of system operation.

2.1.1 Control Switch Panel

2.1.1.1 System Reset

Function: Reset processor registers to their initial state, with the exception of the M register.

Operation:

1. Data or instructions in core storage are not affected.
2. Reset is active in all modes of operation except run mode.
3. In single step mode, it is necessary to be at T7 time to prevent loss of data or instructions when using reset.

2.1.1.2 Program Stop

Function: Causes a level 5 interrupt for the console. With appropriate sub routines, this stop is used to cycle down the processor and I/O devices to a stop.

CAUTION

If these routines are not in the program, use of the program stop key may cause loss of information.

Operation:

1. The program stop key is pressed and a level 5 interrupt is developed.
2. The 0 position of the console keyboard device status word is a 1, indicating to the program that a program stop is requested.
3. A user-supplied programmed wait loop is required to block mainline operations until the operator intervenes.
4. The interrupt routine should allow the program to continue when the start key is pressed.
5. If an overlapping or malfunction operation such as printing or moving disk data is being performed, the program operation must be completed or data and operating system integrity can be destroyed. These factors must be considered in the levels-program-stop interrupt routine.

2.1.1.3 IMM Stop

Function: Stops the processor immediately. Interrupt and cycle stealing occur at T7 of the cycle in which the IMM Stop occurs.

Operation:

1. Data from I/O devices can be lost if the devices can be operating at the time of the IMM Stop.
2. A complete program restart is required.

2.1.1.4 Program Start

Function: Causes the program to start or continue from its present state. The program continues according to the setting of the mode switch.

Operation:

1. If a program start routine is in the program and the start key is pressed following completion of a program stop operation, the instruction being processed continues as though no program stop had occurred.
2. If the start key is pressed after reset, the instruction specified by the instruction counter (normally zero) is the first one executed. By using the load IAR function and entering a new instruction address, a different starting address can be manually inserted after reset each time the start key is pressed.
3. In the load or display modes the instruction address register is advanced each time the start key is pressed.
4. When in single step, single memory cycle, or single instruction mode, the processor advances a single increment of the specified mode each time the start key is pressed.

2.1.1.5 Load IAR

Function: In the load mode position, data entered in the bit switches is loaded directly into the instruction address register via the storage buffer register.

Operation:

1. The key is functional only when the processor is in the load or display mode.
2. When in the load mode, an address set in the bit switches is entered in the instruction address register when the load IAR key is pressed.
3. Display: When in this mode, the contents of the B register enter the IAR when the load IAR key is pressed.

2.1.1.6 Program Load

Function: Provides a means for entering a program into the system.

Operation:

1. Paper Tape System
   a. Pressing the load key causes groups of 4, four-bit characters (16 bit words) to be loaded into core consecutively, beginning at location zero.
   b. Groups continue to be read until a punch in the fifth channel is encountered.
   c. When a punch in the fifth channel is encountered, loading stops and control transfers to word zero.
2. Card Read Punch System
   a. Pressing the key causes a card to advance from pre-read through the read station.
   b. The contents of each column are stored consecutively in storage locations beginning at location zero.
   c. The 12 bits are split into five operation bits and eight displacement bits, two of which are sign bits.
   d. At completion of the card cycle, an automatic branch to 0000 is executed.

Note: If the card reader is installed, program load is not active on the paper tape.

2.1.1.7 Console/Keyboard

Function: Sets bit position 3 in the keyboard/printer device status word (DSW) to indicate to the program that the keyboard is the source of input data during program control.

Operation: In the console position, the bit switches are the source of input data. In the keyboard position, the keyboard is the source of input data.

2.1.2 Mode Switch

Rotary switch to control mode of machine operation.

2.1.2.1 Load

Function: Provides for manual entry of data or instructions from the bit switches to core storage or I register.

Operation:

1. In load mode, operation of the load IAR key transfers bit switch data (2-15) to the I register.
2. When in load mode, pressing the start key enters the bit switch data (0-15) into core storage at the address indicated in the I register. The I register is incremented by 1.

3. Switching from load to any other mode of operation does not affect storage or result in reset of any set conditions.
4. During machine operation, IMM stop or program stop keys must be pressed prior to switching to load mode to preserve the integrity of the data in core storage and to preserve the program.
5. It is not necessary to reset prior to switching to load mode. Such switching does not affect any set conditions other than the B register.

2.1.2.2 Display

1. *Function:* To display the data at any location in core storage.

   Operation: In display, pressing of the start key displays, in the B register, the data at the address specified in the I register prior to pressing of the start key.

   Pressing the start key successively displays sequentially increasing addresses. That is, the I register is incremented each time the start key is pressed.

2. *Function:* Load the I register with the contents of the B register.

Operation: Depressing the load IAR key transfers the B register contents into the I register.

2.1.2.3 Run

Function: To condition the system for the start of programmed operation.

Requirements:

1. Pressing the start key in run mode results in program operation beginning at the address specified by the I register.
2. Pressing the IMM stop key halts machine processing at the end of the active cycle at T7 time.
3. Switching from run mode to any other mode requires IMM stop or program stop prior to switching to insure integrity of the core data.

2.1.2.4 Interrupt Run (INT RUN)

Function: Forces a level five interrupt after completion of each instruction.

Operation:

1. A level 5 interrupt occurs after the end of each instruction execution.
2. Higher level interrupts are handled automatically during this operation.
3. An interrupt-run program which stops on the level 5 interrupt and starts with the start key is required to use this mode of operation effectively.

2.1.2.5 Single Step (SS)

Function: Pressing the start key advances the processor one clock cycle (T7 to T0, T0 to T1, etc.).

Operation:

1. Pressing the start key in this mode causes a T (X), phase A, pulse to be generated. Releasing the start key causes a T (X), B pulse.
2. Pressing the reset key in a single step mode causes loss of storage integrity unless the clock is in time T5, T6 or T7 and a program integrity unless in T7 time.

Note: The single step mode of operation cannot be used to check the operation of a cycle steal device. The results obtained from this type of operation are not valid and of no use in trouble analysis.

2.1.2.6 Single Machine Cycle (SMC)

Function: Advances the processor one complete machine cycle (T7 to T7) under control of the start key.

Operation: Pressing the start key causes one machine clock cycle.

2.1.2.7 Single Instruction

Function: To advance the processor one complete instruction at a time under control of the start key.

Operation:

1. Pressing the start key causes a complete instruction to be executed.
2. I/O operations are completed to the point of interrupt request.
3. Switching to another mode of operation does not affect instructions or data.

2.1.3 Console Bit Switches

Function: Provide for manual entry of a machine language instruction or binary data into core storage, an instruction address in the I register, or manual control by program interrogation.

Operation:

1. Data set in the bit switches can be loaded into core storage under program control.
2. When the machine is in load mode, the contents of the bit switches are gated directly into the core storage location addressed by the I register.
3. The bit switches have no effect on the processor under any other mode except as addressed by an I/O command.

2.1.4 CE Panel

2.1.4.1 Storage Load Switch

Function: Provides a starting point for isolating problems and checking the storage circuits.

Operation: Data, as set up in the bit switches, cycles through all of core storage. Setting this switch allows cycling of memory by turning on the run controls and incrementing the I register.

2.1.4.2 Storage Display Switch

Function: Provides for checking the core storage circuits.

Operation: The core storage contents are displayed in the B register console lights in a sequential manner. Setting this switch allows core storage to cycle by turning on the run controls and incrementing the I register. A parity error results in an immediate halt if the parity run switch is off.

2.1.4.3 Non-Storage Load and Cycle Switches

Function: Allows console data (bit) switches to be used as a source of data in place of core storage.

Operation: With non-storage load and cycle (NSLC) switch on, the input and output to core storage is crippled. Input to the B register comes from the bit switches (or I/O Bus as a result of an Execute I/O instruction).

An operation may be entered and executed from the bit switches, either in single step, single instruction, SMC, or run modes. If a valid operation code is entered and the mode switch is in run, the 1131 cycles through the operation code, incrementing the IAR and cycling again. This permits scoping of I cycles, E cycles and controls without disturbing the contents of storage. If an invalid operation code is entered, it is decoded as a wait command and the 1131 stops.

Example #1:

1. Machine fails on any long instruction. By single stepping on a double word instruction, it is found that there never is an I-2 cycle.
2. a. Turn on the NSLC switch.
   b. Turn the mode switch to run.
   c. Set load accumulator long instruction in the bit switches (hex C400).
   d. Press the start key. The 1131 cycles and the I-2 circuits may be scoped dynamically for the failure.

Example #2:

In order to examine an XIO instruction and IOCC in single step or single machine cycle mode, the following technique may be used:

1. Turn on the NSLC switch.
2. Turn the mode switch to single machine cycle.
3. Set up XIO instruction in the bit switches (hex 0800).
4. Step through the I1 cycle to the E1 cycles by pressing the start key.
5. Change the bit switches to the desired IOCC word, i.e. device, function codes.
6. Step through the E1 cycle.
7. Turn off all bit switches and press the start pushbutton.
8. If the function of the IOCC was a sense command, the DSW is brought into the A register. If the device had been a 1442, with a feed command, a card would have fed from the hopper, etc.

2.1.4.4 Interrupt Delay

Function: Blocks Interrupts.

Operation: The interrupt delay switch, when on, inhibits setting of the interrupt request circuits.

2.1.4.5 Parity Run

Function: Provide a means of bypassing the error when an out-of-parity character is read out of core storage.

Operation: When the parity run switch is in the on position, errors do not stop the system. When the parity run switch is in the off position, the system stops at the end of the cycle in which the error is detected.

CAUTION

This switch must be returned to the off position before the system is returned to the customer.

2.1.4.6 Lamp Test Pushbutton

Function: Tests all lamps and SCR lamp drivers to see if they are in good condition.

Operation: Pressing the lamp test switch lights all indicator lamps.

2.1.5 Miscellaneous Switches

2.1.5.1 Power On/Off

Function: Provide for removing or applying power to the entire system. When off, 24 vac is still up and the convenience outlet power is on.

2.1.5.2 Alarm On/Off (SCA Machines only)

Function: This switch is located on the console keyboard and provides a means of turning off the SCA alarm in the CPU, should the program not do so for any reason.

2.1.5.3 Emergency Power Off

Function: Removes power to every unit of system including convenience outlets but not to the primary of the 24 vac supply.

Operation: Requires CE intervention to reset.

2.1.5.4 Power Supply Voltage Potentiometer

Function: Provides ability to set each dc voltage accurately. It can be used to help isolate marginal circuit conditions. Located on each supply.

Operation: Allows a 4% variation of processor dc voltages, one at a time. This is not considered a normal trouble-shooting procedure.

DANGER

The potentiometer is not mechanically stopped to prevent over voltage loss of power.

2.1.6 Indicators

There are two versions of the console indicator panel for the 1130:

1. 1131 machines with serial number 11601 and up and all machines below this serial number with the synchronous communications adapter (SCA) installed.
2. 1131 machines with serial numbers 11600 and lower provided that SCA is not installed.

2.1.6.1 Console

The following is a description of the indicators common to all console indicator panels.

Power On: No single indicator on the 1130 indicates the power-on condition. However, with power on, one or more of the status and/or console indicators light.

Instruction Address Register (IAR) has 16 positions and provides full-time indication.

Storage Address Register (SAR) has 16 positions and provides full-time indication. Positions 1 and 2 are used on machines with 32k and 16k core storage only (models 2 and 3).

Storage Buffer Register (B) has 16 positions and provides full-time indication.

Arithmetic Factor Register (D) has 16 positions and provides full-time indication.

Accumulator Register (A) has 16 positions and provides full-time indication.

Accumulator Extension Register (Q) has 16 positions and provides full-time indication.

Operation Register (OP) has five positions and provides full-time indication.

Operation Flags has flag bit (F5), tag bits (T6 and T7), and modifier bits (M8 and M9).

Condition Register has two positions and provides full-time indication of carry (C) and overflow (O).

Cycle Control Counter has six positions (32, 16, 8, 4, 2, and 1) and full-time indication.

Interrupt Levels has five positions and indicates interrupt level.

Machine Cycle Indicators has seven positions, indicates type of I or E cycle and provides full-time indication.

Clock Cycle Indicators has eight positions, displays T Clock position when in single cycle operation and provides full-time indication.

Special Arithmetic Indicators has six positions and provides full-time indication. The positions are: add, arithmetic control (AC), shift control (SC), accumulator sign (AS), accumulator carry (TC), and zero remainder (ZR).

X7 Clock Indicator has one position, displays X clock 7 when in single cycle operation and provides full-time indication.

Wait is on when CPU is in wait condition.

P1-P2 has two positions, uses parity bits to indicate when the halfword read from core storage is even.

Index Register displays index register address.

2.1.6.2 Consoles with SCA

The following indicators are installed on the console panels for all 1131 machines with SCA, and on machines with a serial number of 11601 and up.

CE Indicators: There are eight CE indicators located in the center section (second row from the bottom) of the display panel. These indicators can be used to indicate circuit conditions as needed. See 2.1.6.3 for an example of their use. The following table shows the terminals that must be wired to activate the CE indicators.

CE Indicator Terminals (with SCA)

Location of Terminals

CE Lamp 1	B-A1A3B13	CE Lamp 5	B-A1A4B13
CE Lamp 2	B-A1A3D13	CE Lamp 6	B-A1A4D13
CE Lamp 3	B-A1A4B12	CE Lamp 7	B-B1M2B13
CE Lamp 4	B-A1A4D12	CE Lamp 8	B-B1M2D13

(RDY) Ready: This indicator lights when the data set is ready.

(ABL) Enabled: This indicator lights when the 1130 program has enabled the adapter to respond to a ring indicator signal from the data set.

(REC) Receive: This indicator lights when the adapter receive trigger is on.

(TSM) Transmit Mode: This indicator lights when the adapter is in the transmit mode.

(BFR) Buffer Loaded: This indicator lights when the buffer contains data which has not yet been read out.

(CLK) Clock Running: This indicator lights when the receive clock is running.

(DI) Data In: This indicator lights when the receive data line from the data set is at a receive space level.

(CP) Character Phase Memory: This indicator lights when the adapter is operating in character phase.

2.1.6.3 Consoles without SCA

The following indicators are used on the 1130 machines with serial numbers of 11601 and lower which do not contain the SCA:

CE Indicators: There are 12 indicating lamps located, two rows of six lamps in the lower portion of the lamp panel. These can be used to indicate circuit conditions as needed. Input to each lamp is shown on ZL101. The input level must be plus to light the indicator.

The lamps do not require an external driver. Therefore, any normal signal level may be used as an input without concern for loading the circuit excessively.

Example:

While stepping through a program, if indication is desired each time the 'accumulator equal zero' flip-flop comes on (KG221), wire CE indicator # 1 to the FF so that it indicates the on condition. To accomplish this, wire B-A1E2B04 to B-A1A3B13.

CE Indicator Terminals (without SCA)

Location of Terminals

CE Lamp 1	B-A1A3B13	CE Lamp 7	B-B1M2B13
CE Lamp 2	B-A1A3D13	CE Lamp 8	B-B1M2D13
CE Lamp 3	B-A1A4B12	CE Lamp 9	B-B1N2D13
CE Lamp 4	B-A1A4D12	CE Lamp 10	B-B1N2B13
CE Lamp 5	B-A1A4B13	CE Lamp 11	B-B1N4B12
CE Lamp 6	B-A1A4D13	CE Lamp 12	B-B1N4D12

2.1.6.4 Keyboard Console

Disk Unlock goes off with a cartridge in place and the disk motor switch ON.

Disk Ready is on when the heads are loaded. Indicates power on and disk drive ready.

Run is on with the CPU in run mode and the start key pressed.

Parity Check is on with the recognition of a parity error; either halfword read out of core storage is even and the parity is not on.

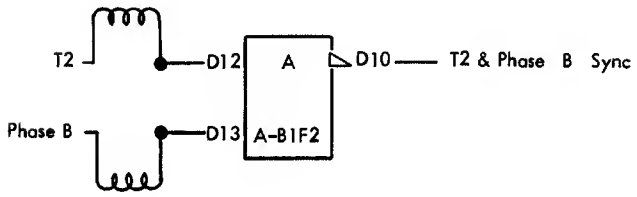
Keyboard Select is on when a request for keyboard interrupt has been serviced and the keyboard is ready to operate.

Forms Check is on if the console printer is out of paper.

Numeric Shift is on when the keyboard is in the numeric mode. This indicator is not present on machines with SCA installed or serial numbers of 11674 and up.

Alpha Shift is on when the keyboard is in the alpha mode. This indicator is not present on machines with SCA installed or serial numbers of 11674 and up.

1. Place T2 time into one leg on a CE AND circuit by jumpering B-A1D4B2 to A-B1F2D12.
2. Condition the other leg on the AND circuit with phase B by jumpering B-A1C4J10 to A-B1F2D13.
3. The sync output is taken off at A-B1F2D10 as a minus pulse.



2.2 CE MAINTENANCE CARDS

Three SLT cards are available for use in maintaining the 1130 system.

1. The CE card which is included with the machine.
2. The CE indicator latch card (part 5801358) which is optional, and must be ordered by the CE.
3. The 12 position indicator card (part 5803975). Refer to logic diagram AD002 for use of this card.

2.2.1 CE Card

A CE card has been furnished in location A-B1F2. The card contains six circuits which can be used as minus ORs or plus ANDs. Each circuit may be wired, by using jumpers, as needed to aid in diagnosing problems or setting up multiple conditions for syncing a scope. Two or more circuits may be wired together to form a latch, etc., for diagnostic purposes.

Example # 1:

The CE desires to sync the oscilloscope on B phase of T2 time.

Example #2:

In some cases of highly intermittent failures, it is desirable to have a circuit to monitor circuit conditions at the time of the failure.

On logic page XR291, there are several lines that give a read error. In the case of an intermittent failure, watching each line on an oscilloscope would be a tedious job.

The CE may wire a circuit monitor to do this watching for him (Figure 2-1).

When the input to the latch goes negative, the latch turns on and the second OR block inverts the minus output from the AND block for a plus input to the CE indicator lamp. The latch remains on until the reset key is pressed. When the indicator comes on, the line giving the read error has been found. The reset leg may be wired to a plus voltage level so that the latch cannot be turned off by the operator. In this manner, an error condition is indicated as long as power is not turned off.

Note: Other single cards can also be used in location A-B1F2.

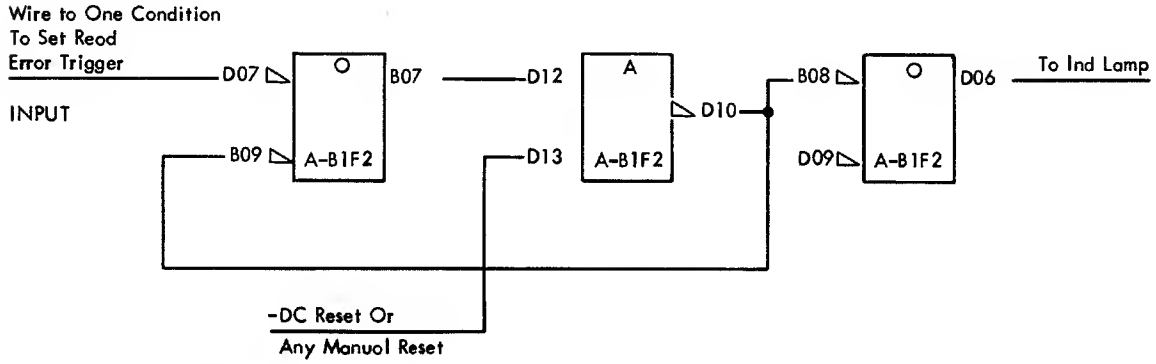


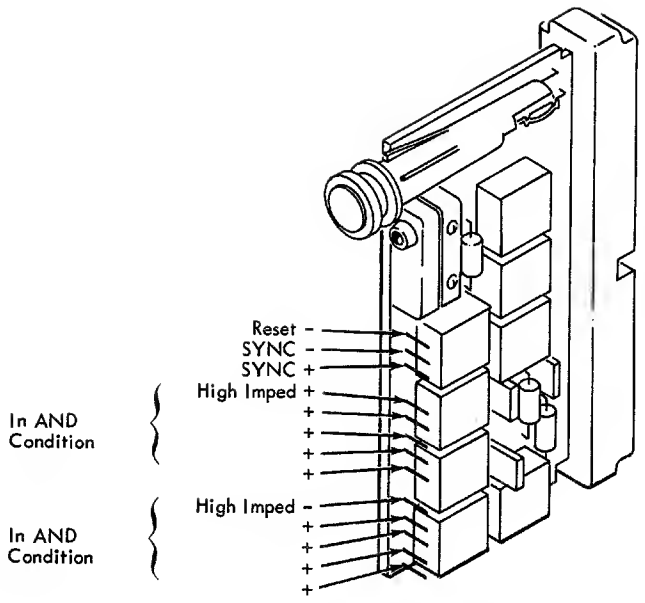
Figure 2-1. Circuit Monitor

2.2.2 CE Indicator Latch Card (Figure 2-2)

An optional CE indicator latch card (part 5801358) is available from Mechanicsburg as a troubleshooting aid for SLT machines. Thirty-three inch jumpers (part 4203785) with SLT connectors for use with the latch card and replacement lamp assembly (part 5711078) are also available, as needed.

The CE latch is a 2-12 SLT card which plugs into the pin side of the SLT board. It can be plugged into any two vertically adjacent locations *except* edge connectors. The card is intended for use in socket locations with no discrete wiring; however, with care, it can be used in socket locations with no more than one discrete wire wrap on any pin. If the card is left on the SLT board for extended lengths of time, normal machine vibrations may cause it to work out on the pins and lose contact.

Plugging the card into the board provides voltages (+3, -3, +6) and ground only. The card was designed for use with medium and high speed SLT circuits which require +3 volts on pin D03.



PART 5801358

DANGER

Slow-speed circuits have +12 volts on pin D03. If there is any doubt, measure pin D03 with a voltmeter or scope.

CAUTION

The card must be plugged in with the lamp on top and the modules on the right. If the card is plugged in upside down or in the card side of the board, circuit damage may result.

The CE latch has an indicator bulb, a reset switch, a reset line, plus and minus sync points for scope triggering, and two 5-legged AND blocks ORd to turn on the latch. Inputs are brought to the card by jumpers.

Note: If only one input to an AND block is to be used, it must go to the high impedance input. If two or more inputs are used, one must go to the high impedance input. These high impedance inputs are so designed that the CE latch is not set if the input is floating.

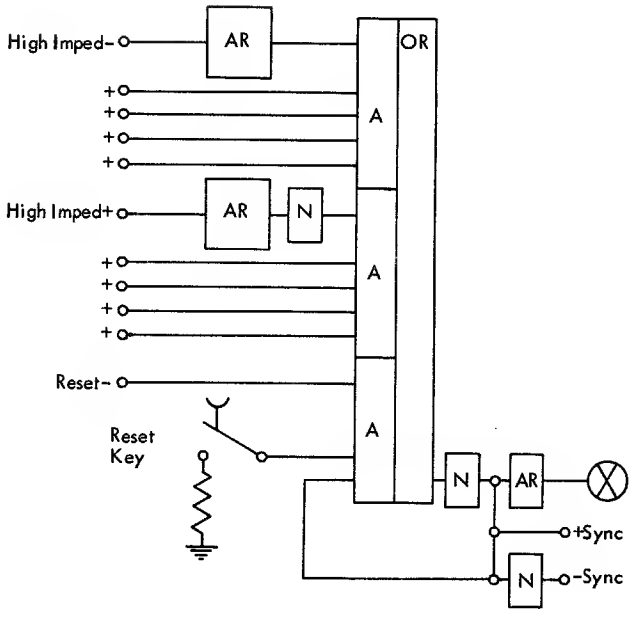


Figure 2-2. CE Indicator Latch Card

The CE latch can be used in a variety of ways. Some of them, with examples, are listed below:

1. *Baby Sitter* To find out if several inputs are all plus at the same time, plug the card into the pin side of the SLT board and jumper the suspected lines to one of the AND blocks. Be sure that one of the jumpers goes to the high impedance input. If all the lines go plus together, the latch will turn on and light the indicator. Reset the latch by pressing the reset button on the card.
2. *Meter or Scope Substitute* A scope may show a line at or near ground level which may or may not be floating. Jumper the line to the appropriate high impedance input. If the line is floating, the latch will *not* set. If the line is not floating, the latch will set.

3. *One-Time Pulse Detection* If a line should not change during a particular sequence of events, jumper the line to the appropriate high impedance input. For example, if the line is plus and should never go to minus, jumper it to the minus high impedance input. If the line changed value or had a pulse on it, the latch will turn on.
4. *Scope Sync Point* The necessary signal lines for the syncing condition can be jumpered to one of the AND blocks. Jumper a reset signal, such as a clock pulse, to the reset line on the card. The latch will then turn on with the ANDing conditions and turn off under control of the reset line, furnishing a stable sync point. The scope sync lead is plugged into the plus or minus sync point on the latch card.
5. *Temporary Fix* Turn the latch on and reset as described in item 4. Use either the plus or minus sync output to condition circuit requiring the temporary fix.

2.3 CONSOLE PRINTER AND KEYBOARD

The printer is mounted to allow a 90 degree rotation for access to the base of the printer. Printer signal and power cables can be disconnected by the CE for problem isolation and replacement. The printer is capable of OLSA operation for installation test out and off line maintenance when feasible. The keyboard is mounted such that tilting does not affect contacts or adjustments. The CE can disconnect the keyboard signal cable for isolation.

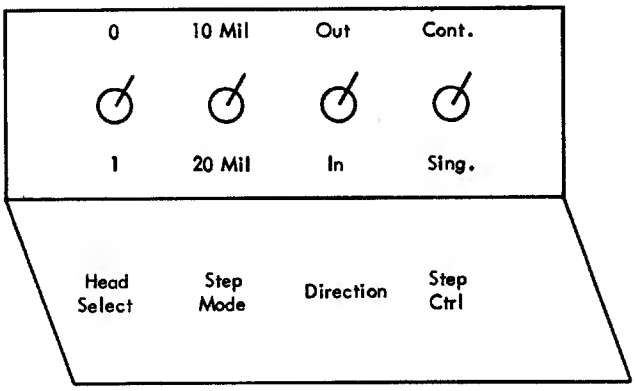
2.4 DISK STORAGE (1131 Models 2, 3, and 4)

The disk storage drive can be taken off line by disconnecting the signal cable. The CE switches function only when the disk drive is off line. Operation of the 1131 CPU is not affected when the disk drive is off line. The disk storage adapter provides modulo 4 checking of write and read data. The access location must be verified by the program. The disk storage is basic to all 1130 Models 2, 3, and 4.

2.4.1 Controls

2.4.1.1 CE Switches

The CE switches located on the back of the drive are inoperative when the machine is on line. When the signal cable is disconnected, the drive is placed in read select mode of operation and the disk storage may be controlled by the switches.



Head Select: This toggle switch allows the CE to select either head as input to the read circuit.

Step Control: This switch is of the momentary contact type when moved in the single direction. The carriage makes one step each time the switch is operated in the single direction.

The step control switch locks the carriage into a continuous stepping mode when operated and causes the carriage to step continuously at a 15 ms rate. This operation is particularly useful when performing adjustments on the two access control SLT cards.

Stepping Mode: This switch controls the number of tracks moved for each actuator step. When in the 10 mil position, each step of the carriage moves the heads one track position. When in the 20 mil position, each step moves the heads two track positions.

Direction: This toggle switch allows the CE to select the direction of carriage movement when stepping. Select forward when motion toward the spindle is desired, and reverse when the opposite direction is desired.

More details on the diagnostic procedures for the disk storage may be found in the IBM FEMM *Single Disk Storage (Serial 00000-39999).*

2.4.1.2 Disk On/Off

Function: Provides for removing or applying ac power to the disk drive unit.

Operation:

1. Controls the drive motor.
2. Provides, indirectly, the head load and unload facility.

2.4.2 Indicators

The indicators for the disk storage drive are located on the keyboard console (refer to paragraph 2.1.6.4).

2.5 1442 CARD READ PUNCH, MODELS 5, 6, AND 7

All operational checks on the 1442 must be performed on-line. Punch and read error checking is performed in the adapter. The DSW provides error indication to the program and lights on the 1442 provide indication to the operator. Data read or punch errors drop ready on the 1442 but do not stop the system except by program control. Any error stops the 1442 operation and signals the program by the DSW.

2.5.1 Controls

This section describes the switches on the 1442 and their functions.

2.5.1.1 CE Switch

The CE switch controls the ac power to the 1442 so that mechanical adjustment may be made while the system power is up.

2.5.1.2 Start Key

To run in:

1. Turn power switch on.
2. Check that the card path is empty.
3. Place cards in the hopper.
4. Press the start key to feed one card.
5. The ready light comes on. To restore the machine to ready status after manual stop, press the start key.

2.5.1.3 Stop Key

Removes the machine from ready status.

2.5.1.4 Non-Process Runout Key

This key causes cards to be ejected from the card path without being processed. The key is ineffective unless the reader punch is removed from ready status and the hopper is empty.

2.5.2 Indicators

The following is a description of the indicators on the 1442.

2.5.2.1 Power On Light

Indicates that the ac and dc power is applied to the reader punch control circuits.

2.5.2.2 Ready Light

Indicates that the reader punch is prepared to accept instructions from the processing unit. The following conditions are required.

1. Power must be on.
2. Cards are registered at the read station.
3. Cards are in the hopper.
4. Stacker is not full.
5. Check light is off (no card jam or feed failure conditions).
6. Chip box is not full or removed.

2.5.2.3 Check Light

Indicates that one of the following error conditions displayed on the backlighted panel has occurred. Any one of these removes the 1442 from the ready status.

1. Hopper – Indicates that a card failed to feed from the hopper.
2. Read Station – Indicates a read station jam or a defective phototransistor or lamp.
3. Punch Station – Indicates a jam at the punch station.
4. Transport – Indicates a jam in the stacker transport area.
5. Feed Clutch – Indicates that the clutch failed to latch up thus causing an extra feed cycle to be taken.
6. Read Registration – Indicates the first two readings of each card hole were not equal during the read cycle.
7. Punch – Indicates that the punch echo data did not equal the punch data.

The check light, along with the corresponding error condition, is turned off by the following action:

1. Remove jammed cards, if any, from the card path with the CE switch turned off.
2. Mispositioned card, or read, or punch error – run out cards with NPRO key.

2.5.2.4 Chip Box Light

Indicates that the punch chip box is full or has been removed.

2.6 1132 PRINTER

All operational checks on the 1132 must be performed on-line. Error checking is done in the attachment circuits. Error indication is provided to the program by the DSW, and to the operator by lights on the 1132.

2.6.1 Controls

The manual controls provide manual operation of some printer functions which are independent of the program. The indicators provide visual indication of printer functions.

2.6.1.1 Power On/Off

This switch controls power to the main printer drive motor and to the 48 volt magnet supply.

2.6.1.2 Start Key

Initiates the printer ready status.

2.6.1.3 Stop Key

Takes the printer out of ready status at the completion of the current program step.

2.6.1.4 Carriage Space Key

Pressing of the key single spaces the printer paper carriage. This key functions only when the printer is in not ready status.

2.6.1.5 Carriage Restore Key

Restores the paper carriage to the hole in channel #1. This key functions only when the printer is in not ready status.

2.6.1.6 Carriage Stop Key

Stops the carriage immediately and takes the printer out of ready status on completion of the current program step.

2.6.1.7 CE Switch

Controls ac power to the main printer drive motor and to the 48 volt magnet supply.

2.6.2 Indicators

2.6.2.1 Power On

The light on indicates that system power is on and logic voltages are available to the 1132.

2.6.2.2 Ready

Light comes on with power on, forms in place, and start key pressed.

2.6.2.3 Form Check

Indicates need for more paper forms on the printer.

2.6.2.4 Print Scan Check

Set when printer cycle steal cycles are taken before the program has completely set up the print scan field.

2.7 1627 PLOTTER

2.7.1 Controls

The plotter controls provide manual operation of plotter functions independently of programming. The plotter controls are mounted on front panel of the 1627.

2.7.1.1 Power On/Off

The power on/off switch connects 115 volts ac from the P5 connector on the rear of the recorder to the cooling fan and the power supply transformer. A neon indicator, located directly below the switch, is lighted whenever the switch is on.

2.7.1.2 Carriage Fast Run

The carriage fast run switch allows the pen carriage to be stepped rapidly to the left or right at the rate of 120 steps per second. The switch may be used to move the carriage to any desired area of the graph, or for operational checkout of the carriage control circuits and the carriage step motor.

2.7.1.3 Carriage Single Step

The carriage single step switch allows the pen carriage to be moved in single step (1/100") increments either to the left or right. This control, in combination with the drum single step control, permits the operator to accurately align the carriage on a point or fixed coordinate on the graph.

2.7.1.4 Chart Drive On/Off

The chart drive on/off switch allows the operator to disable the front and rear chart takeup motors. This permits the use of single sheets of graph paper in place of the paper rolls.

2.7.1.5 Pen Up/Down

The up/down switch provides a means of manually raising and lowering the pen from the surface of the drum.

When the recorder is first turned on, or if the pen is removed and replaced when the pen is in the up position, the pen can remain down. When this occurs, turn the switch first to the down position, then to the up position.

2.7.1.6 Drum Fast Run

The drum fast run switch allows the drum to be stepped rapidly up or down at the rate of 120 steps per second. The switch is used in the same manner as the carriage fast run control to move the pen to any desired area of the graph, or for operational checkout of the drum control circuits and the drum step motor.

2.7.1.7 Drum Single Step

The drum single step switch allows the drum to be moved in single step (1/100") increments either up or down. This control, in combination with the carriage single step control, permits the operator to accurately align the pen on a point or fixed coordinate on the graph.

2.7.1.8 Carriage Scale Factor Adjustment (Model 2 Only)

A carriage travel scale factor adjustment is provided for the purpose of varying the carriage travel to compensate for stretch or shrinkage in the graph paper.

2.7.2 Indicators

There are no indicators for the 1627 Plotter.

2.8 1134 PAPER TAPE READER

Operational checks must be performed on-line.

2.9 1055 PAPER TAPE PUNCH

2.9.1 Controls

This section describes the controls for the 1055 Paper Tape Punch.

2.9.1.1 Feed Key

Pressing the feed key energizes the punch clutch to punch successive feed holes.

2.9.1.2 Delete Key

Pressing the delete key energizes the punch clutch and all interposer magnets (except channel 8) to punch a delete character.

2.9.2 Indicators

There are no indicators for the 1055 Paper Tape Punch.

2.10 STORAGE ACCESS CHANNEL

There are no switches, indicators, or controls associated with SAC.

2.11 SYNCHRONOUS COMMUNICATIONS ADAPTER (SCA)

2.11.1 Controls

This section describes the controls for the Synchronous Communications Adapter (SCA).

2.11.1.1 STR/BSC Switch

This toggle switch in the STR position places the adapter in the STR mode of operation. In the BSC position the adapter operates in the binary mode.

2.11.1.2 Speed Selection Switch

This rotary switch is set to establish the number of bits per second which may be transmitted or received, as determined by the data set, and the type of remote terminal with which communication is taking place. This switch also has a single-pulse position for CE use.

2.11.1.3 Single Cycle Pushbutton

This pushbutton switch is used by the CE to aid in maintaining the adapter. With the speed selection switch in a position other than single pulse, pressing the pushbutton starts a cycle of one bit duration. With the speed selection switch in the single pulse position, pressing the pushbutton steps the SCA clocks one position. The pushbutton must be pressed a total of 32 times to step through one bit time in the single pulse mode.

2.11.1.4 CE Mode Switch

The CE mode switch, which is used by the CE in maintaining the adapter, must be turned off for normal adapter operations. This switch must be on, however, to allow the single cycle pushbutton and the space/mark switches to function.

When using the CE mode switch, note that:

1. The SCA adapter is reset when CE MODE is turned off.
2. No interrupts occur when in CE mode. Also, interrupts are inhibited (CE Single-Shot) during the reset caused by turning the CE mode switch off (item 1).
3. CE mode is effective in single pulse and all baud rates.
4. Test/operate switch should be at TEST for off-line operation.

CE Mode of Operation: The intent is to provide a service technique that allows the customer to operate his system while the SCA is being serviced. Basically, all diagnostics should be run to completion or programmed termination to determine the failing function. Exercise the failing function in CE mode if possible to accomplish the repair.

Note: Ensure that CE single-shot is adjusted as specified on logic AD000.

Jumpers can be installed to alter the mode of operation as follows:

Jumper Number	Purpose	Jumper Connection	Logic
1	Off-line	H4D07-H4D08	FC111
2	Force receive-mode	L5B07-E3B10	FC411
3	Force transmit-mode	L5B07-E3B08	FC411
4	Allow interrupts in diagnostic mode (note 1)	L5D07-L5D08	FC411
5	Allow continuous clock-run	H5B12-G4D11	FC111
6	Receive line data in CE mode (note 2)	C6D04-C6B05	FC411

Note 1: Jumper 4 is required to run the display-function test.

Note 2: Set mark/space switch to SPACE when using jumper 6.

Note 3: Remove all jumpers when testing is complete.

Procedures:

1. *Transmit.* Install jumpers 1 and 3. Use single cycle and mark/space switches to shift character at any baud rate.

   For continuous transmitting, install jumper 5 and press single cycle pushbutton.

   With a data set connection, data from the idle-sync register can be transmitted to another 1130 in CE-receive mode or normal-receive mode, or to other STR/BSC devices in receive mode.

   System RESET, if pressed, terminates the transmit operation. Press the single-cycle pushbutton to continue.

2. *Receive.* Install jumpers 1 and 2. Use single cycle and mark/space switches to simulate receiving the character in the idle-sync register. To establish character phase, match the idle character once for STR, twice for BSC. Establish data phase with a non-matching character (buffer light turned on indicates data phase).

   For continuous receiving, install jumper 5 and press the single cycle pushbutton. All 1's in idle-sync register and mark/space switch set to MARK allows scoping of the character phase and preceding circuits.

   To receive from the line, remove jumper 1 and add jumper 6 (2 and 6 installed). In this mode, data from the line can be used to establish character phase. Be sure that mark/space switch is set to SPACE.

2.11.1.5 Space/Mark Switch

This switch is effective only when the CE mode switch is on. It determines the level of the incoming data line, simulating a 1 being received when set to the mark position and a 0 when set to the space position.

2.11.2 Indicators

The indicators for the SCA are on the Console Indicator Panel (refer to paragraph 2.1.6.2).

2.12 2501 CARD READER

The 2501 Card Reader is used on the 1131 Models 2 and 3. Operational checks must be performed on-line. Read error checking is performed in the adapter. The DSW provides error indication to the program, and lights on the 2501 provide indication to the operator. Data read errors drop ready on the 2501 but do not stop the system except by program control. Any error stops the 2501 operation and signals the program by the DSW. The 2501 requires the 208 vac 60 Hz Feature on 1131 Models 2A and 2B.

2.12.1 Controls

This section describes the switches on the 2501 and their functions in 2501 operations.

2.12.1.1 Normal On/CE Mode Off Switch

The normal on/CE mode off switch, on the power supply cover, must be in the normal on position while the 2501 is operating with the system. When the switch is set on CE MODE OFF, the ac voltage is disconnected from the:

1. Drive motor.
2. DC power supply (+2.5 and +24 volts).
3. Process meter.

2.12.1.2 Start Key

To run in:

1. Turn power switch on.
2. Check that the card path is empty.
3. Place cards in the hopper.
4. Press the start key to feed one card.
5. The ready light comes on.

To restore the machine to ready status after manual stop, press the start key.

2.12.1.3 Stop Key

Removes the machine from ready status.

2.12.1.4 Non-Process Runout Key

This key causes cards to be ejected from the card path without being processed. The key is ineffective unless the reader punch is removed from ready status and the hopper is empty.

2.12.1.5 Lamp Test Switch

The lamp test switch, on the CPU console, activates all of the 2501 operator panel lamp drivers. Burned out lamps are easily located by using this switch.

2.12.2 Indicators

This section describes the indicators on the 2501.

2.12.2.1 Power On Light

Indicates that the ac and dc power is applied to the reader control circuits.

2.12.2.2 Ready Light

This light indicates that the 2501 is ready to accept instructions from the CPU. The following conditions must be satisfied for the ready light to be on:

1. Power on.
2. Cards in hopper, except during last card sequences.
3. Card in preread station, except during last card sequences.
4. Neither of the following error conditions on:
   a. Feed Check.
   b. Attention.
5. Machine not stopped with stop key.

2.12.2.3 Feed Check Light

This light is turned on when a card is mispositioned in the card path or when certain equipment malfunctions occur. When turned on by a mispositioned card, the feed check light can be turned off with the following procedure:

1. Empty the hopper.
2. Raise the machine cover.
3. Clear the card path of all cards.
4. Close the machine cover.
5. Press the nonprocess runout key.

The feed check light turns off the ready light.

2.12.2.4 Read Check Light

This light indicates that a card is sufficiently mispositioned to impair reading. The light is turned off by pressing the NPRO key.

2.12.2.5 Attention Light

This light indicates an open cover or a full stacker. The light is reset by correcting the condition. The attention light turns off the ready light.

2.13 1231 OPTICAL MARK PAGE READER

The 1231 Optical Mark Page Reader is attached to the 1131 Models 2 and 3. Operational checks are performed with the 1231 on-line. Error checking is performed in the adapter circuits. Error indication is provided to the program by the DSW, and to the operator by lights on the 1231. The 1231 requires the 208 vac 60 Hz Features on 1131 Models 2A and 2B.

2.13.1 Controls

The controls on the 1231 provide manual operation of some 1231 functions which are independent of the program.

2.13.1.1 Start Key

A depression of the start key feeds the first data sheet and establishes continuous running conditions with two exceptions:

(1) If the feed mode switch on the 1231 is set to continuous, the feed circuits are interlocked with the program of the processing system and will not feed the first sheet until the processing system is placed in an operating status, and (2) if the reader is in a load program cycle, the program control sheet feeds and the control bits are stored.

2.13.1.2 Stop Key

A depression of the stop key halts document feeding and lowers the hopper plate to facilitate the loading of more data sheets.

2.13.1.3 Reset Key

A depression of the reset key raises the hopper to the feed position and resets the electronic circuitry. Check or error conditions should be corrected before pressing the reset key.

2.13.1.4 Program Load Key

A depression of the program load key clears the delay line storage of previously stored data, and conditions the machine for program loading. This key is lighted during the program load cycle.

2.13.1.5 Master Mark Switch

The master mark switch is active only on machines equipped with the master mark special feature. This switch controls the capability of the optical mark page reader to recognize a master mark on the right edge of the data sheet. When this switch is on, the recognition of a master mark causes the data in the first ten positions of storage to be cleared and new master-mark data to be accepted.

2.13.1.6 Feed Mode Switch

The feed mode switch has two settings: continuous and on-demand. When the switch is set to CONTINUOUS, documents feed continuously. This setting requires the processing unit program to give a read instruction within 150ms after buffer full in the 1231. Buffer full can occur as frequently as once every 1585 ms. When the switch is set to ON-DEMAND, feeding is controlled from the system program. The next document will not feed until the contents of the delay line (from the previous document) is transferred to the computer.

2.13.1.7 Check Length Switch

Three check-length switches are located on the operator's panel, one for each of three sets of switches associated with fields. These switches have two settings: segment and word. The setting defines the length of the item as it will be checked for each field. The segment setting will check the five positions of a segment; the word setting will check all ten positions of a word.

2.13.1.8 Select Condition Switches

Each of the three select switches has four settings: off, no mark, multi-mark, and other-than-one. Each switch is associated with a check-length switch and one of the three fields. The settings represent the conditions in a given field under which a document will be directed to the select stacker.

2.13.1.9 Read Mode Switches

Switches for Mark Discrimination: These three switches, each associated with a set of field-checking switches, determine the conditions of mark discrimination. Each read mode switch has four settings: single response, multiple response, single response-select uncertainties, and multiple response-select uncertainties. See Mark Recognition and Discrimination in this publication for a detailed description of each switch setting.

Control Timing Marks Switch: This switch enables the 1231 to eliminate the 75 ms delay associated with the timing-mark checking feature. The switch has two settings, yes and no. YES is used when the documents to be processed have the six extra control-timing marks needed for IBM 1230 operation. NO is used when no control timing marks are on the documents; the 75 ms delay is eliminated.

2.13.1.10 Timing Mark Check Switch

This switch is an 11-position rotary switch with settings numbered 0 through 9 and off. The switch is preset by the operator to match the units-position count of timing marks on the data sheets to be processed. For example; if there were 106 timing marks on a document to be processed, the switch would be set at 6.

2.13.2 Indicators

The indicators provide visual indications of 1231 functions.

2.13.2.1 Start Key Light

The start key, when lit, indicates that the machine is in a ready state. The light goes off when the start key is pressed, and the light remains off until the machine is again conditioned to the ready state.

2.13.2.2 Feed Check Light

This light indicates a sheet jam, a misfeed, a double-sheet feed, a full stacker, or an empty hopper. These conditions cause the machine to stop, and the condition must be corrected before the light can be turned off by pressing the reset key.

2.13.2.3 Process Check Light

This light indicates the following conditions:

1. A parity error in storage logic.
2. The count of data-sheet timing marks is not in agreement with the setting of the timing-mark switch.
3. Failure of processing unit to take data from the B-reg before the A-reg loaded new data into it. See 1231 Data Flow.
4. A logic or delay line failure when:
   a. No control bits are loaded into the master line during the reading of a program control sheet.
   b. No data bits are loaded during the reading of a data sheet. (Blanks normally load a C-bit.)

Note: On the 1231, the process check light also turns on if the number of timing marks on the detail data sheet does not equal at least the number of words programmed to read by the program control sheet.

2.13.2.4 Read Light

This light indicates that the read head lamp is burned out or weak. If depressing the reset key does not turn off the read light indicator the read head lamp should be replaced.

2.13.2.5 System Stopped Light

This light is turned on whenever the processing system is stopped while connected to the 1231.

2.13.2.6 Refeed Select Document Light

This light comes on whenever one or more of the following conditions occurs (the last document in the select stacker must be reprocessed):

1. A multi-mark is detected during the reading of the master-mark document.
2. An uncertainty is detected during the reading of the program control sheet.
3. An uncertainty, without an accompanying dark mark, is detected during the reading of the master-mark sheet.
4. A read instruction during continuous mode operation is received too late.
5. A process check occurs and a new sheet has started to feed (in continuous feed mode only).

Intentionally Blank

Section 1. Basic Machine

3.1 APPROACH TO SCHEDULED MAINTENANCE

The prime objective of any maintenance activity is to provide maximum availability to the customer. Every scheduled maintenance operation should assist in realizing this objective. Unless a scheduled maintenance operation cuts machine downtime, it is unnecessary.

Note: Do not adjust or disassemble a unit that is working properly, even if tolerances vary from specification.

3.1.1 Visual Inspection

Visual inspection is the first step in every scheduled maintenance operation. Always look for corrosion, dirt, wear, cracks, binds, burnt contacts, and loose connections and hardware. Alertness in noticing these items may save later machine downtime.

3.1.2 Electronic Circuits

Diagnostic programs are the basic tools used in scheduled maintenance of the 1130 system.

Do not adjust pulses unless the condition of the machine **warrants it.**

3.1.3 Mechanical Units

The three basic scheduled maintenance steps performed on every mechanical or electromechanical machine are clean, lubricate, and inspect. Remember not to do more than recommended scheduled maintenance on equipment that is operating satisfactorily.

3.1.4 Scheduled Maintenance Procedures

The Scheduled Maintenance Chart (Figure 3-1) lists details of scheduled maintenance operation. During normal scheduled maintenance, perform only those operations listed on the chart for that scheduled maintenance period. Observe all safety practices.

3.1.5 Console Printer Preventive Maintenance

The *Keyboardless I/O Printer FE Maintenance Manual* covers preventive maintenance for the console printer.

CODE U	CODE R	LOCATION OPERATION	FREQ.	OPERATION
0		FILTERS & CONSOLE LIGHTS	1	Check for dirty filters. Clean or replace as required. Check cooling fans for proper operation. Check console lights.
2		CONSOLE PRINTER		For detailed information refer to FEMM I/O Printer (Modified IBM Selectric ® form #225-3207.
8		TESTS	4	Run diagnostic tests and meter verification test.
9		MISC.	6	Inspect for loose terminal board connections on SLT panels. Check ground connections. Check line cord for safe condition and proper grounding. Depending on keyboard useage check operation and lubrication of the keyboard.
7		POWER SUPPLIES	12	Check line voltage and power supply voltages at SLT large boards. Check cables and wiring for loose terminals and overheated insulation.

Figure 3-1. Scheduled Maintenance Chart

3.1.6 Console Keyboard Preventive Maintenance

Figure 3-2 and 3-3 cover preventive maintenance for the console keyboard.

3.1.7 Disk Storage Preventive Maintenance

The *FE Maintenance Manual, IBM Single Disk Storage (Serial 00001-39999)*, covers preventive maintenance for the disk storage drive.

Area	LUBRICATION CHART Item	IBM Lubricant	Freq-uency (Manths)
Keyboard	A sharp painted instrument (large needle or scribe) is useful in lubricating with **IBM 6. Avoid using excess oil.**		
	Key stem at bellcrank and retaining wire	# 6	6
	Key stem bellcrank pivats	# 6	6
	Permutation bar pivat	# 6	6
	Bail contact pivats	# 6	6
	Permutation bar at bail stop plate	# 6	6
	Restaring magnet armature pivat		6
	Haak channel at paints af cantact with latch pull bar	#22	12
	Restaring bail where it cantacts latches	#22	12

Figure 3-2. Lubrication Chart - Keyboard

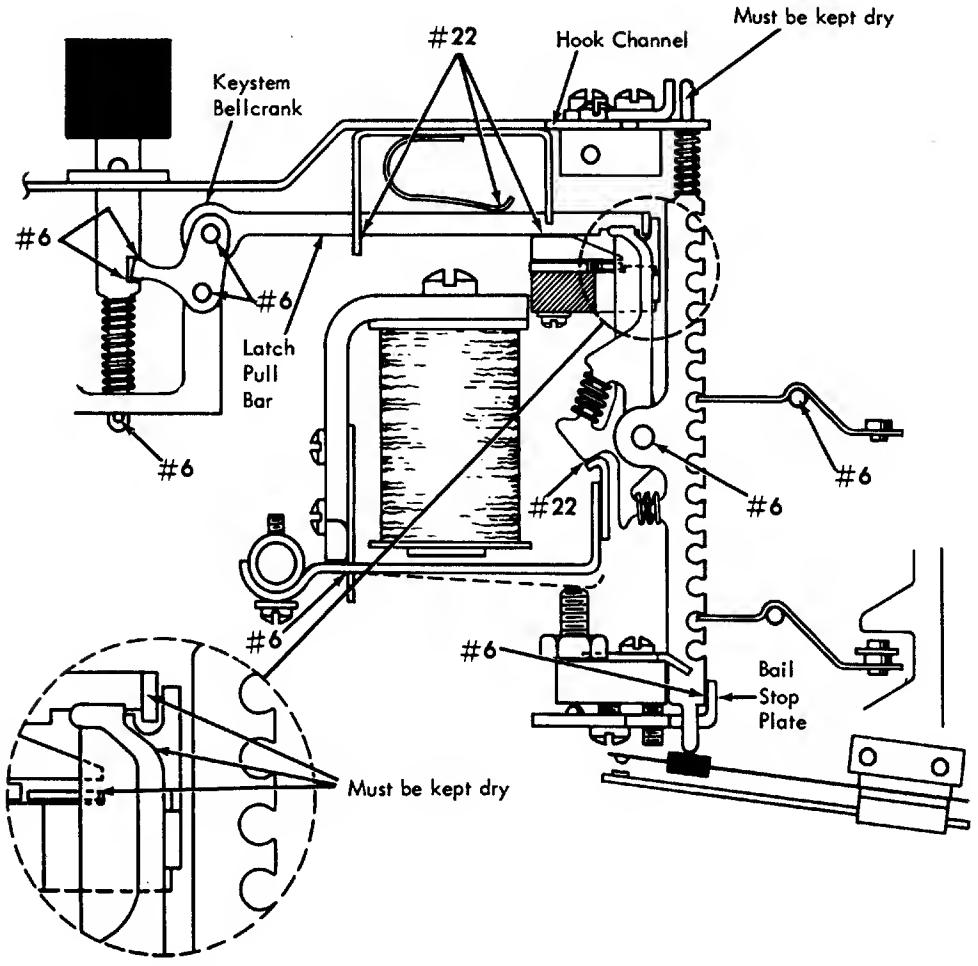


Figure 3-3. Keyboard Lubrication

3.2 PREVENTIVE MAINTENANCE OF I/O DEVICES

3.2.1 1132 Preventive Maintenance

The FE Maintenance Manual for the 1132 Printer contains detailed information.

3.2.2 1442 Preventive Maintenance

The FE Maintenance Manual for the 1442 describes preventive maintenance of the 1442.

3.2.3 1134 Preventive Maintenance

The FE Maintenance Manual for the 1134 describes preventive maintenance of the 1134.

3.2.4 1055 Preventive Maintenance

The FE Maintenance Manual for the 1054/1055 describes preventive maintenance of the 1055.

3.2.5 1627 Preventive Maintenance

The FE Instruction-Maintenance Manual for the 1627 describes preventive maintenance of the 1627.

3.2.6 Storage Access Channel

Preventive maintenance for this feature is determined by and accomplished through the devices attached to it.

3.2.7 Synchronous Communications Adapter

This feature is installed in the 1131 machine, and requires the same preventive maintenance procedures as the other logic gates.

3.2.8 2501 Card Reader

The FE Maintenance Manual for the 2501 describes preventive maintenance of the 2501.

3.2.9 1231 Preventive Maintenance

The FE Maintenance Manual for the 1231 describes preventive maintenance of the 1231.

Intentionally Blank

Section 1. Basic Machine

4.1 SOLID LOGIC TECHNOLOGY MAINTENANCE

All normal maintenance procedures for solid logic technology components are found in *IBM Field Engineering Manual of Instruction, SLT Packaging.* This manual includes information regarding:

Wrapped wire connections.
Crimped connections.
Soldered connections.
Wiring change procedures.
SLT service tools.
SLT card maintenance.
Measurements.
Ventilating systems.
SLT components and packaging.
SLT service techniques.

4.1.1 SLT Cards

The lettering within a logical block on a systems diagram page gives the location of that block in the card gates. It also indicates other pertinent data as described in the SLT Packaging FEMI. Identification of pins, panels, rows, and columns is shown in the SLT Packaging FEMI.

Logic block locations within the system diagrams are shown on system diagram card location charts.

The system diagram index gives the machine features indexing of ALDs and maintenance diagrams.

4.1.2 Single Shots

The single shots are adjusted with the CE alignment screwdriver, part 460811, or jewelers screwdriver, part 2108286.

Always refer to logic page AD000 for the current timing and tolerance of single shots.

Adjust each of the single shots so that the time from the input pulse to the output pulse is equal to the time specified for the individual single shot.

4.2 CORE STORAGE UNIT

Note: The 1131 Model 4 with a cycle time of 5.85 μs uses the 3.6 μs core storage.

CAUTION

Be extremely cautious when working around core storage. Do not disturb the core planes. Do not leave the core storage unit unattended when the covers are removed.

4.2.1 Removal

1. Remove all power to the system.
2. Remove bottom bracket from board.
3. Unplug the connecting assemblies (on the wiring side of the large board), using pulling tool, part 2108860, by pulling straight out.
4. Unlock the four screws that secure the array to the large board.

Note: Pull out straight to prevent damage to pins and land patterns on the core unit.

5. Remove core array from machine and place array in a safe and secure working area.

CAUTION

Do not leave the unit unattended as the connections and pins can be damaged. Do not place unit with pins down as the outside pins may be bent as array is picked up.

4.2.2 Adjustment Procedure for 3.6 Microsecond Core Storage

The 3.6 microsecond storage unit has three potentiometers which must be adjusted to optimize storage performance.

These potentiometers set the reference voltage level (array current magnitude), position the sense amplifier strobe, and set the sense amplifier sensitivity.

The core storage voltage adjustments, reference voltage adjustment, sense amplifier strobe adjustment, and sense amplifier sensitivity adjustment are given on SD013 (sheets 2 through 5). Sheet 1 of SD013 contains a summary of the adjustments for the 3.6 microsecond (SJ-4) core storage.

4.2.2.1 Core Logic Voltage Adjustments

Check and adjust (if required) the logic voltages for core storage, using the Weston 901 (or equivalent) meter. The voltage limits and test points are given in adjustment procedure I on SD013 (sheet 2).

4.2.2.2 Sense Control Adjustment

Check and adjust (if required) the sense control voltage, using the Weston 901 (or equivalent) meter. The voltage limits and test points are given in procedure II on SD013 (sheet 2).

4.2.2.3 Strobe Adjustment

Scope setup using differential input:

1. Channel 1 and 2 set on AC INPUT and 0.02v/div.
2. Invert channel 2.
3. Vertical mode switch set to ADDED.
4. Input to channels 1 and 2 are twisted pair wires (part 2182907) connected to bit-6 sense lines.
5. Sweep set to 0.5 microseconds/division and x10 magnification.
6. Sync + DC external on '+ read cycle'.

Adjustment:

1. Set the bit switches to all ones and turn on the storage load switch. This causes the CPU to load all ones into all core addresses.
2. Perform adjustment procedure IlI on SD013 (sheet 3 of 5).

4.2.2.4 V-Reference Adjustment

Load the core storage with the core adjustment diagnostic test (PID 03A6), which contains a worse-case pattern program. After the pattern is loaded, the program stops.

Using the maintenance switches, set the system in automatic display mode and parity check. In this mode, the CPU cycles through the storage at the maximum speed (continuous read/write) and regenerates the data read out. If parity errors are detected, the processor stops and displays a parity check.

If the core adjustment test cannot be loaded, set an alternating bit pattern into all core storage locations with the bit switches. Make the required core adjustments. After the adjustments are made, load the core adjustment test and remake the adjustments.

The parity is restored at the faulty location by:

1. Note the address in the M register.
2. Set the mode switch to LOAD.
3. Press the load IAR switch.
4. Set the bit switches to the correct word.
5. Set the storage load switch to ON, and the display switch to OFF. Set run and storage load switches to OFF, and the display switch to ON.
6. Press the start switch.
7. Set the mode switch to RUN and the storage load switch OFF, display switch ON.
8. Press the start switch. The processor should again cycle through storage without errors.

It should be noted that VSA-VE varies if the -3v supply is varied; but once adjusted, it remains at the optimum value of operation even if -3v is varied. It is suggested that the adjustment procedure described below should be used after every card replacement.

SLT voltages -3, +3, +6, and the special voltage, +12v, should be set to within 1% of their nominal values as measured at the core storage large board with the system operating. Always use the Weston 901 (or equivalent) meter when adjusting core storage values.

CAUTION

Do not use a scope for this adjustment as the reference is to -3v, not ground. Load the core adjustment test. With the processor running, perform adjustment procedure IV on SD013 (sheet 4) using the Weston 901 (or equivalent) meter.

Note: Restart the core adjustment test program (PID 03A6) after each failure.

4.2.3 Adjustment Procedure for 2.2 Microsecond Core Storage

The storage unit contains three potentiometers which must be adjusted to optimize storage performance.

These potentiometers set the reference voltage level (array current magnitude) and position the sense amplifier strobe. Load the core storage with the core adjustment diagnostic test (PID 03A6), which contains a worse-case pattern program. After the pattern is loaded, the program stops. Using the maintenance switches, set the system in automatic display mode and parity check. In this mode, the CPU cycles through the storage at the maximum speed (continuous read/write) and regenerates the data read out. If parity errors are detected, the processor stops and displays a parity check.

If the core adjustment test cannot be loaded, set an alternating bit pattern into all core storage locations with the bit switches, make the required core adjustments. After the adjustments are made, load the core adjustment test and remake the adjustments.

The parity is restored at the faulty location by the following procedure:

1. Note the address in M register.
2. Set the mode switch to LOAD.
3. Press the load IAR switch.
4. Set the bit switches to the correct word.
5. Set the storage load switch to ON, and the display switch to OFF. Set run and storage load switches to OFF, and the display switch to ON.
6. Press the start switch.
7. Set the mode switch to RUN, the storage load switch to OFF, and the display switch to ON.
8. Press the start switch. The processor should again cycle through storage without errors.

It should be noted that VSA-VE varies if the -3v supply is varied; but once adjusted, it remains at the optimum value of operation even if -3v is varied. It is suggested that the adjustment procedure described below should be used after every card replacement.

SLT voltages -3, +3, +6, and the special voltages, +12v, -15v, and Vz should be set to within 1% of their nominal values as measured at the core storage large board with the system operating. Always use the Weston 901 (or equivalent) meter when adjusting core storage voltages.

4.2.3.1 Strobe Adjustment

Refer to SA022 for this adjustment.

4.2.3.2 V-Reference Adjustment

Refer to SA022 for this adjustment.

4.3 OSCILLATOR

The frequency of the oscillator in the 1131 is not adjustable. The frequency of the 1131 oscillator is 2.25 MHz (±11.25 kHz) in machines with the 3.6 microsecond core storage (1131 Models 1, 2, and 4) and, is 3.64 MHz (±18.16 kHz) in machines with the 2.2 microsecond core storage (1131 Model 3).

4.3.1 2.25 MHz Oscillator Phase Adjustment for 3.6 us Core Storage

Objective: Set up initial adjustment when oscillator is replaced.

Adjustment:

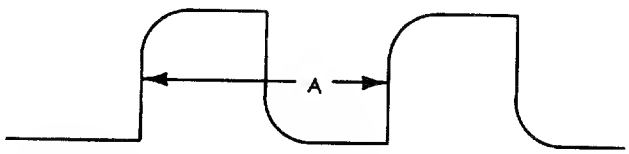
1. Set the mode switch to RUN and the CE switch to STORAGE DISPLAY, and press the start key.
2. Sync on + oscillator trigger, B-A1C4D13 (KA101).
3. Display + A Phase, B-A1CAJ05 (KA111) and + B Phase B-A1C4J10 (KA101).
4. Adjust pot on card (B-A1E5) (KA101) for 450 nanosecond/cycle for both A and B phases (Figure 4-1). Refer to AD000.

4.3.2 3.64 MHz Oscillator Phase Adjustment for 2.2 us Core Storage

Objective: Set up initial adjustment when oscillator is replaced.

Adjustment:

1. Set the mode switch to RUN and the CE switch to STORAGE DISPLAY and press the start key.
2. Sync on + oscillator trigger, B-A1C4D13 (KA101).
3. Display + A Phase, B-A1C4J05 (KA111) and + B Phase B-A1C4J10 (KA101).
4. Adjust pot on card (B-A1E5) (KA101) for 275 nanosecond/cycle for both A and B phases. Refer to AD000.



A=0.450 us ± 0.045 us (3.6 us machines)
A=0.275 us ± 0.028 us (2.2 us machines)

Figure 4-1. Oscillator Phase

4.4 CONSOLE KEYBOARD

4.4.1 Keyboard Removal

To remove the keyboard for servicing:

1. Unlock table top and tilt to the front (screwdriver in slot under left end of table top).
2. Remove four nuts on welded studs.
3. Raise and tilt back cover, switches and lights.
4. Remove four screws, and keyboard is free for service.
5. To remove keyboard from machine disconnect paddle connectors.
6. Assemble in reverse order.

4.4.2 Keyboard-Printer Single Shots

Objective: Set up initial adjustments of single shots when they are replaced.

Adjustment:

1. Load and execute a printer ribbon shift loop from the diagnostics.
2. Sync on + X1O Write, A-C1H7B04 (XW101).
3. Display the outputs of the printer single shots, A-C1F5B03 and A-C1F5B07 (XW101).
4. Adjust pots on cards for pulse width specified on AD000.

Note: If keyboard single shots are to be adjusted, perform items 5, 6, and 7.

5. Interchange keyboard single shots, A-C1E3, (XK101) with printer single shots, A-C1F5 (XW101).
6. Adjust as in item 4.
7. Replace cards.

4.4.3 Keyboard Assembly

4.4.3.1 Contacts

Keyboard contacts should be inspected for air gap, tension, and contact rise. Check contact surfaces for nodes and pits caused by burning. Insufficient air gap in latch contacts can cause false error indications. Note the condition of these contacts, particularly if the keyboard has been jarred or dropped.

4.4.3.2 Adjustment

Bail Contacts: With bail contact assemblies out of the machine, form each contact strap to require a pressure of 9 grams to 11 grams to close points (measure at contact point). Position the contact plates for contact air gap of 0.018 inch to 0.028 inch with all latch assemblies restored (Figure 4-2).

Latch Contacts: Form the operating strap to require 18 grams to 24 grams pressure to close contacts. Measure at contact pad. Pivot contact assembly mounting bar to obtain 0.018-inch to 0.028-inch contact air gap across the unit. Stationary contacts may be formed for individual air gap.

Restoring Bail Contacts: Form the operating strap to require 48 grams to 52 grams of pressure to open the contacts.

Position the contact bracket for 0.007 minimum to 0.015 maximum clearance between the movable strap and the operating insulator disk on restoring bail. It is very important to have clearance between the contact strap and the disk. After all restoring-magnet adjustments are made correctly, restoring-bail contacts should have a minimum of 0.010-inch air gap when restoring magnets are energized.

Note: It is important that restoring bail contacts open before the latch or bail contacts.

Key Stem Contacts: The n/o contacts should have a 1/32-inch minimum air gap. The n/c contacts must open with the minimum pressure of 15 grams at the end of the strap and with minimum movement (1/64 inch) of stationary strap when opening.

1. When the keyboard restore key is pressed 3/32 (±1/64) inch, the upper contact must break. Further depression of 1/32 inch will cause the lower contact to make.
2. ALPH key contact must close when the key is depressed 3/32 (±1/32) inch. If the operator's palm strikes the ALPH key, increase the contact air gap.
3. The NUM contact must open when the key is depressed 3/32 (±1/64) inch.

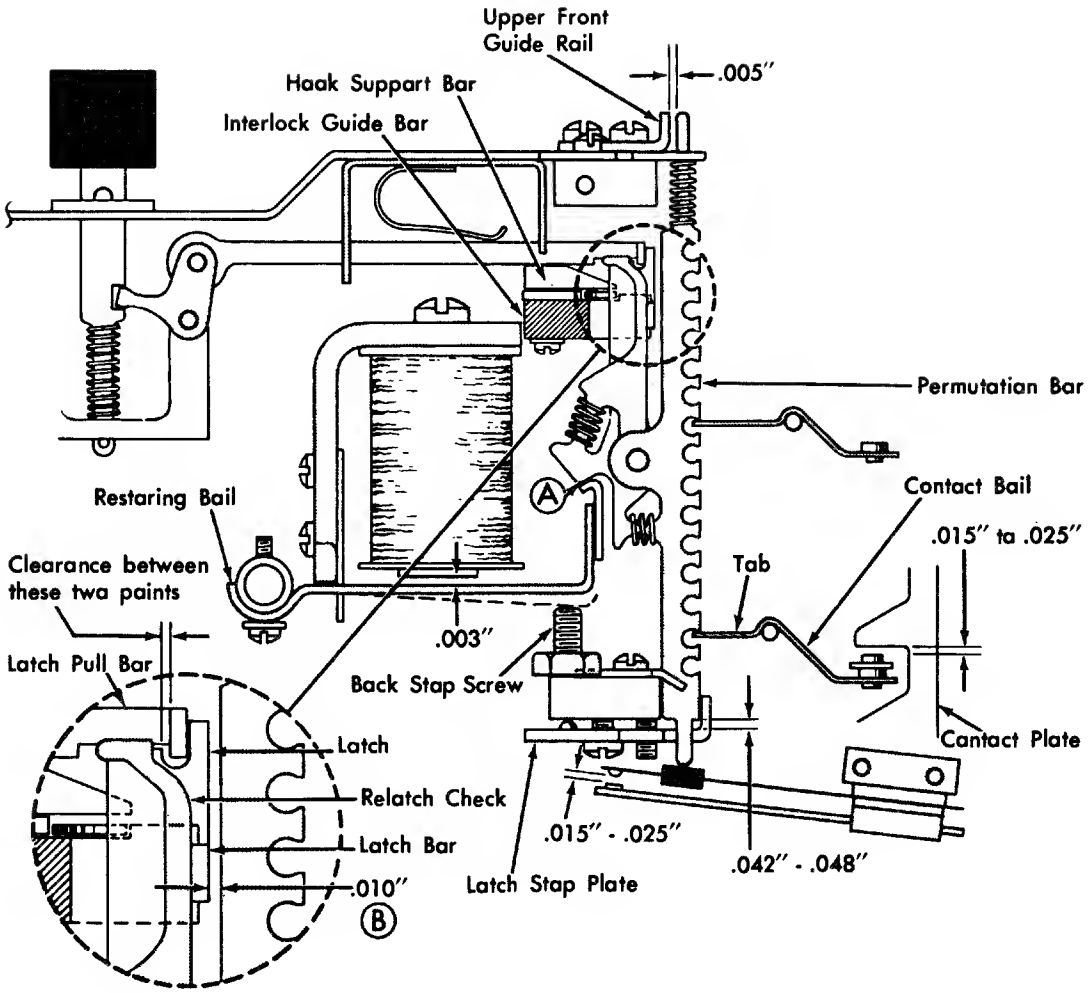


Figure 4-2. Keyboard Adjustment

Contact Bails: When a new bail (Figure 4-3) is installed, form all tabs on each bail for zero to 0.005-inch clearance to associated operation ears on permutation bar, with latch assemblies in restored position. This may be checked on a keyboard with its covers removed. Check tension required to just open a closed bail contact for each key operating that bail. Tension should be at least 15 grams. Bail-contact air gap and tension on operated strap affects this tension and should be checked before a measurement is attempted.

Hook Support Bar: Adjust the four setscrews positioning the latch stop plate to allow bars to drop 0.042 inch to 0.048 inch. Measure on a bar near each holding screw. To measure, lay a 6-inch rule across the top of the permutation bars. If the bar whose travel is to be measured is lower than the 6-inch rule, measure this amount and add it to the 0.042 inch to 0.048 inch given above. Trip the latch and measure the distance that the top of the bar is below the edge of the rule.

Permutation Bar: Adjust the four setscrews positioning the latch stop plate to allow bars to drop 0.042 inch to 0.048 inch. Measure on a bar near each holding screw. To measure, lay a 6-inch rule across the top of the permutation bars. If the bar whose travel is to be measured is lower than the 6-inch rule, measure this amount and add it to the 0.042 inch to 0.048 inch given above. Trip the latch and measure the distance that the top of this bar is below the edge of the rule.

Restoring Magnet:

1. With all latch assemblies restored, insert 0.003-inch gage between armature and magnet core and hold them sealed. Position magnet brackets evenly until restoring bail meets all latches at A, Figure 4-2. This should result in 0.010-inch maximum over-travel of latching point with gage removed.
2. With magnets de-energized, adjust the two backstop screws for clearance between each armature and its magnet core of 0.030-inch, measured at the center-line of core. (Use special 0.030-inch gage issued to measure clearance between feed and idler roll on this machine.)
3. Check adjustment of permutation bar travel and adjustments 1 and 2 by tripping, one at a time, several latches across the unit. Clearance between closest tripped latch and restoring bail should be at least 0.002 inch. Remake adjustments if this condition is not present.
4. Adjust restoring bail pivots so that the restoring bail operates freely but has a minimum of clearance in the pivots.

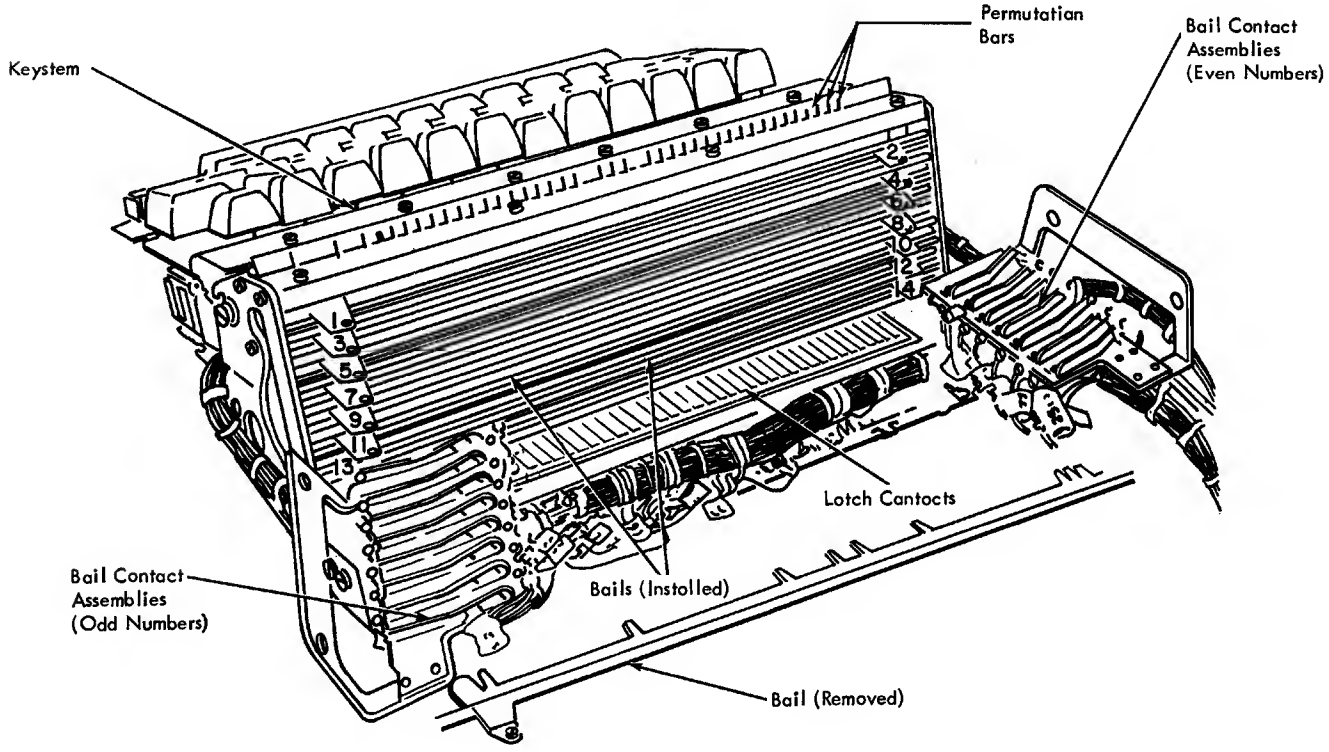


Figure 4-3. Keyboard Permutation Unit - 1

Upper Permutation Support: Note that die-cast supports are not adjustable.

1. Loosen the two end screws in the upper front guide rail and the four screws holding the switch mounting plate comb.
2. Position the comb for 0.010-inch (±0.005-inch) clearance between latch bar and permutation bars (B, Figure 4-2).
3. Position upper front guide rail evenly for 0.005-inch clearance to permutation bars.

Key Unit:

1. Loosen the four screws that hold the key unit to the permutation unit.
2. With key plate level, and with no interlocks (Figure 4-4) affected, a 50- to 80-gram weight on any key top except erase field, NUM, ALPH, and the space bar, must be sufficient to trip its latch assembly. The key must return to its normal position with a 10-gram minimum weight resting on the key top, when its latch assembly has been previously restored.
3. With key plate level, and with no interlocks affected, a 75- to 100-gram maximum weight on the space bar must be sufficient to trip its latch assembly. The bar must return to its original position with a 10-gram weight resting on it when its latch assembly has been previously restored.
4. With key plate level, and with interlocks affected, 90-grams maximum weight on any key top described in 2 above must be sufficient to trip its latch assembly.
5. NUM, and ALPH keys must travel 0.125 with 50- to 80-grams key pressure.
6. With any latch assembly dropped, no hook should slip off its latch when its key top is struck a quick sharp blow with the finger.

Note: Do not oil or grease the hook ends of the latch pull bars. On reassembly, check clearance of latch to pull bar (Figure 4-2).

Key Stem:

1. Remove the nylon retaining wire to free the desired key stem. (Use a follow wire to aid reassembly.)
2. Lift the key from the unit while the end of the latch pull rod is held up and clear of latch. Be careful that the key stem spring does not drop into the unit. Refer to Figure 4-2.
3. Reassemble the unit. Hold the latch pull rod free of the latch and allow the key stem bell crank to rotate into the key stem. Be sure the spring is assembled on the key stem.
4. Test the position for binds.

Contact Bails:

1. Remove the two bail contact assemblies shown in Figure 4-3. Each assembly is held by two screws and may be shimmed away from the side frame.

DANGER

As each bail contact assembly is removed, cover pivot end of contact bails with cellulose acetate tape to keep bails from falling out.

2. Punch a hole in the tape and remove the desired contact bail.

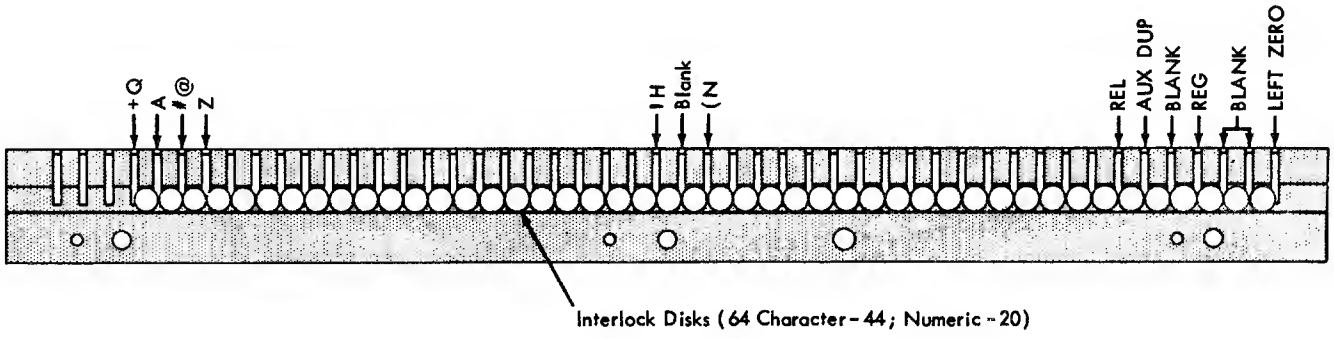


Figure 4-4. Keyboard Interlock Disk

Latch Assembly:

1. Separate the key and the permutation units (Figures 4-5 and 4-6).
2. Remove wires from all stem contacts and the two restoring magnets (Figure 4-6).
3. Loosen the two mounting screws and remove the restoring bail contact assembly.
4. Remove restoring bail by taking out one screw from one of the pivots and turning pivot block away from the armature.
5. Remove the two bail contact assemblies shown in Figure 4-3.
6. Remove the toggle switches from the mounting plate.
7. Remove the contact bails. They are numbered 1 to 15, top to bottom (Figure 4-3).
8. Remove the latch contact mounting bar.
9. Remove the four screws from the latch-stop plate (Figure 4-5).
10. Remove the two springs on the latch assembly to be taken out. The longer spring belongs between the latch and the relatch check lever.
11. Remove the center support screw from the upper latch assembly guide (Figure 4-6).
12. Set the unit on its back. Hold the hook support bar (Figure 4-6) while removing the three screws that hold it. Also, remove the pivot screw.
13. Still holding the hook support bar, set the permutation unit right side up.
14. Slide the hook support bar off, exposing the interlock disks.
15. Lift out the interlock disks adjacent to the latch assembly to be removed. Latch is free to come out of bottom. Note carefully the difference between the release-key latch and other latch assemblies.

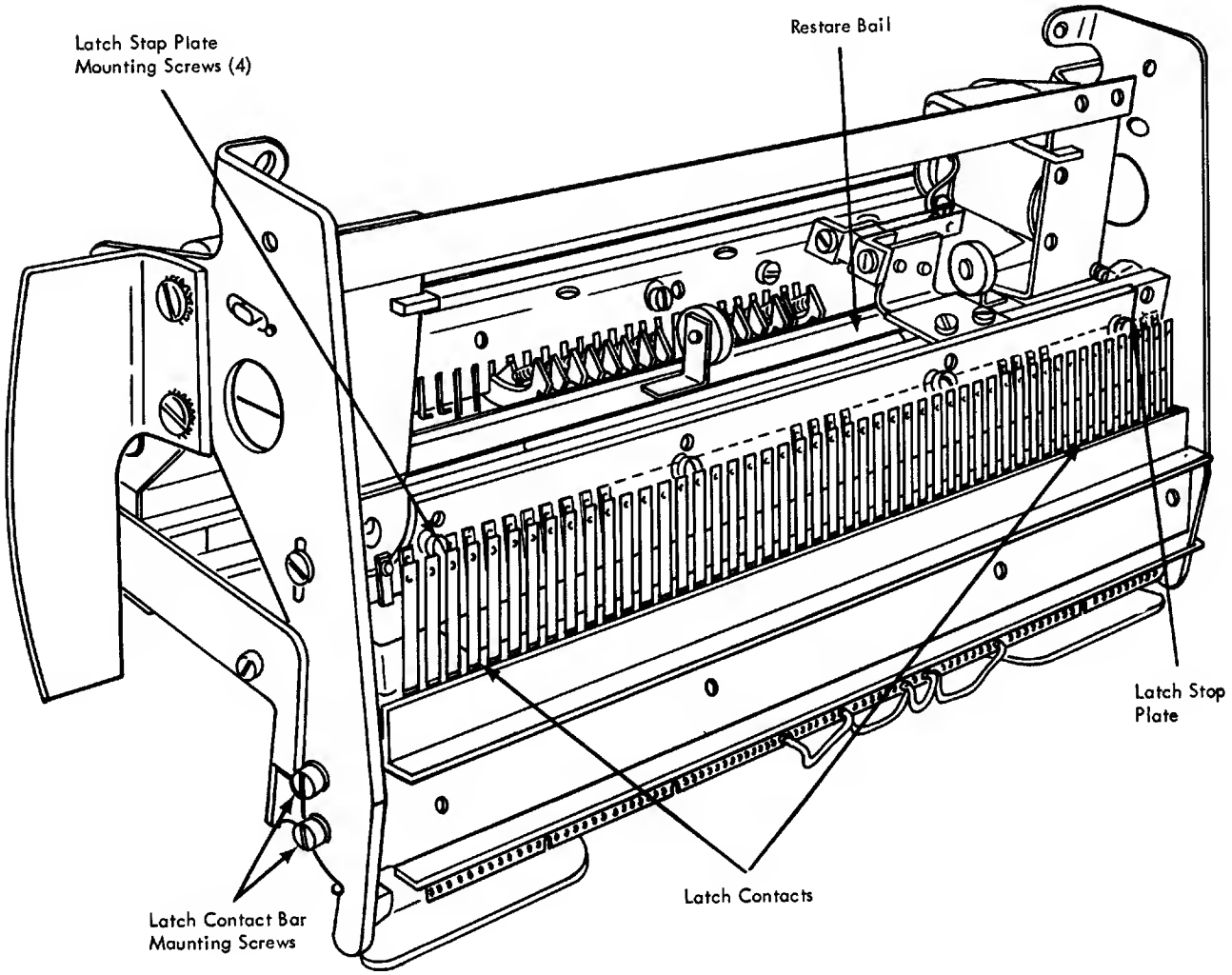


Figure 4-5. Keyboard Permutation Unit - 2

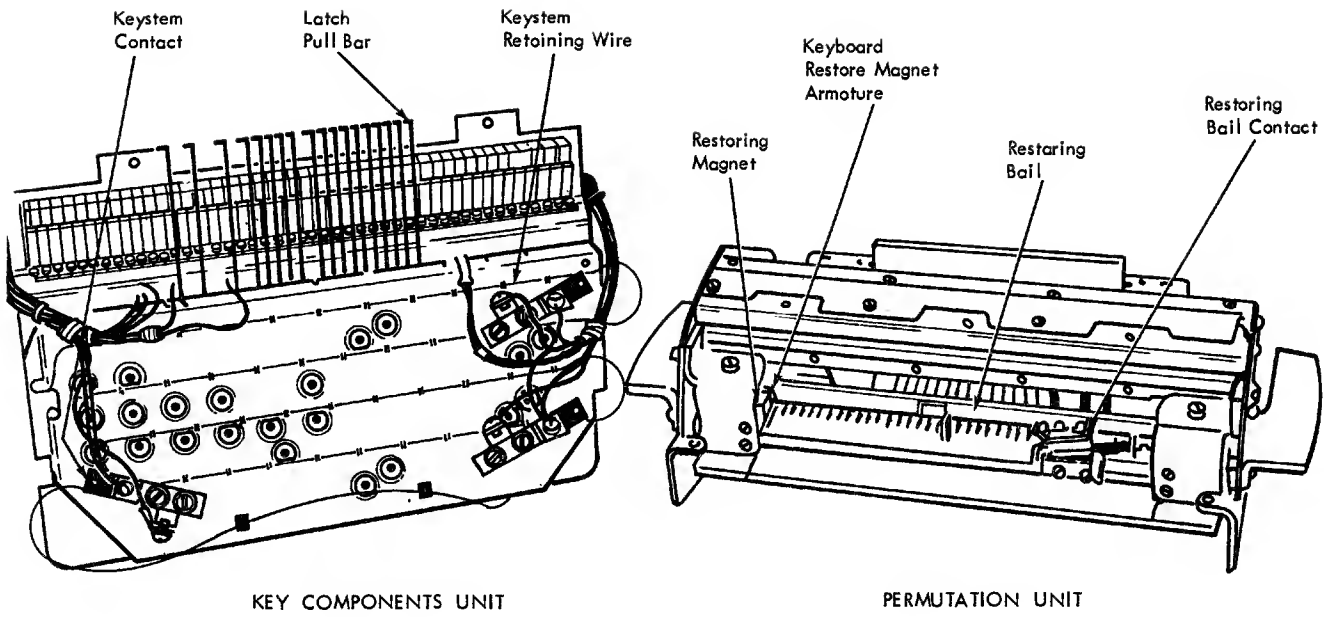


Figure 4-6. Keyboard Permutation Unit - 3

The release-key latch is cut away at the point where the latch would contact the interlock disks. The release key is not interlocked. Figure 4-4 shows the correct position of the 44 interlock disks.

DANGER

When an interlock is removed, all latches tripped off the latch bar can fly out. All parts in direct contact with interlocks, including latches that strike interlocks, must be free of oil or grease.

After reassembly, check all adjustments. When replacing contact bails, stand permutation unit on one end after covering pivot holes with tape to keep contact bails from falling out.

Latch Pull Bar:

1. Separate the key and permutation units; see Key Unit.
2. To replace a pull bar in the top row, remove the key stem in the defective position. If the defective latch pull bar is not in the top row, remove all key stems and the top plate.
3. Remove the defective latch pull bar from the pivot rod (a follower rod will aid in reassembly).
4. Replace the top plate and key stems. Check the clearance of the latch to the pull bar.

4.5 CONSOLE PRINTER

4.5.1 General Information

The console printer used with the 1130 system is an IBM Selectric typewriter modified for data processing equipment. The *Field Engineering Maintenance Manual, I/O Printer (Selectric I/O Keyboardless Printer),* explains all adjustments, lubrication, and maintenance procedures.

The invalid typewriter character (1) prints on any bit combination that does not select a valid character. It does not necessarily indicate incorrect parity.

The motor for the I/O Printer is running whenever the IBM 1130 is turned on, and results in heat drying out the lubrication in the printer. Therefore, the I/O Printer must be lubricated frequently. Lubrication procedures are given in the I/O printer maintenance manual.

4.5.2 Service Checks

To ensure reliable 1130 operation, all typewriter contacts must be carefully adjusted for proper contact air gap, adequate strap tension, and sufficient overtravel when made.

4.5.3 Removal

1. Unlock table top with screwdriver in slot under left front end of table top and tilt back. Remove side covers by removing nut on the front.
2. Slide console printer to the front.
3. Remove covers, if needed.
4. The console printer may now be tilted on its face or back for service, or removed by disconnecting the cables.
5. Assemble in reverse order.

4.6 I/O CABLES

Intermachine power and signal cables for the 1132 and 1442 are attached to the 1131 by means of multiple contact connectors.

Power and signal cables for the console printer and keyboard, 1134, 1055 and 1627 are attached by paddle connectors.

4.7 DISK STORAGE UNIT

Maintenance procedures for the disk storage are described in the *IBM Single Disk Storage (Incremental Access) Field Engineering Maintenance Manual, Form Y26-3668.*

4.7.1 Removal

1. Remove the table top.
2. Remove the top, front, right end and right rear covers.
3. Remove the top cover from the unit.
4. Remove the cartridge.
5. Remove the air duct from rear of the unit.
6. Remove the cable from the switch panel by unplugging it from the TB on top of unit.
7. Remove the dc cable from the TB on the rear of the unit and the ac cable from the sequence box under the right front of unit.
8. Remove four nuts from mounting studs on bottom of the unit.
9. Open the SLT gate.
10. Remove the connector holder.
11. Remove the signal connector from X-A1A2.
12. Remove the signal connector holding clip as the cable leaves box.
13. Remove block from the cable.
14. Pull the cable from the box.
15. Now the unit is ready to be removed. This takes two men, one at the front and one at the rear of the unit. Reach down from the top and lift straight up.
16. Assemble in reverse order.

4.7.2 File Read Write Single Shot

Objective: To delay the start of writing data so that a disk written on one system may be read on another system.

Adjustment:

1. Turn on the disk storage on/off switch.
2. Sync scope on + sector pulse, pin A-C1M6G10 (XF 181).
3. Adjust the potentiometer on card, A-C1M6, so that the single shot output, A-C1M6J13, is negative for the time specified on AD000.

4.7.3 Settle Single Shot

Adjust this single shot as specified on logic AD000.

4.8 MISCELLANEOUS UNITS

4.8.1 Table Top

4.8.1.1 Removal

1. Unlock the table with a screwdriver in the slot under left end of table top and tilt to the front.
2. Remove the two screws on the stay brace.

Note: Do not remove holding screws on the adjustable bracket.

3. Tilt, to the front, the stop bracket on the right end of the table top.
4. Slide the table top to the right and remove.
5. Assemble in reverse order.

4.8.2 Gate Blowers

4.8.2.1 Removal

1. Drop the power with the CE switch.
2. Swing the gates out fully.
3. Remove the mounting screws on the TBs.
4. Remove the two screws on each end of the housing.
5. Swing the housing out and place it on its side.
6. Remove the wires to the fan from the TB.
7. Remove the holding screws.
8. Remove the fan.
9. Place the new fan in position.
10. Assemble in reverse order.

4.8.3 Filters

4.8.3.1 Cleaning

1. Remove the filter by sliding it forward.
2. Clean in clear water.
3. Shake dry.
4. Replace.

4.8.4 Console Lamps

Test the console indicator lamps with the lamp test CE switch: if all lamps fail replace F9.

4.8.4.1 Lamp Removal

1. Drop power.
2. Remove the back cover of console.
3. Pull the bank of lights to the rear.

Note: Be careful not to damage the wires and connectors.

4. Remove the wire terminals from the individual lamp holder.
5. Remove the old lamp from the holder.
6. Replace the new lamp in place and clip the leads.
7. Replace the wire in the holder.
8. Be sure that the leads are not shorted or grounded.
9. Power on.
10. Test the lamps with the lamp test CE switch.
11. Power down.
12. Replace the bank of lamps in the panel.
13. Replace the back cover.
14. Power up.
15. Test the lamps with the lamp test CE switch.

4.8.4.2 Lamp Driver Removal

1. Turn off power.
2. Remove the back cover from the console.
3. Pull the bank of lamps to the rear.

Note: Be careful not to damage the wires and connectors.

4. Remove the lamp terminal from the driver.
5. Remove the signal connector from the driver.
6. Unsolder two leads to bus board and remove driver.
7. Form two outside leads on new driver down at 90 degrees.
8. Place on bus board and solder in place.
9. Replace signal connector on driver.
10. Replace lamp terminal in driver.
11. Turn on power.
12. Test lamps with lamp test switch.
13. Turn off power.
14. Replace bank of lamps in console.
15. Replace rear cover.
16. Turn on power.
17. Test lamps with lamp test switch.

4.8.4.3 SCRID (Silicon Controlled Rectifier Indicator Drivers)

New style indicator drivers, called SCRID, are used on machines with serial numbers 20634 and higher. SCRID machines use SLT modules mounted on circuit boards. The SCRID circuit cards are mounted on the cover at the rear of the console tower. Reference information appears on logic pages ZL101 and ZL111.

4.8.5 Status Indicator Panel

4.8.5.1 Lamp Removal

1. Pull up the lamp cover and remove.
2. Install the new lamp.
3. Replace cover.

4.8.6 Use Meter Single Shot

Adjust this single shot as specified on AD000.

Single shot timings and oscillator-adjustment specifications at the latest engineering-change level are shown on logic page AD000. This page also shows various jumpers and tie-down points.

4.9 1442 CARD READ PUNCH

4.9.1 1442 Attachment Adjustments

4.9.1.1 Read Check Single Shot

Objective: Allow each column of the card to be read twice for read registration checking.

Adjustment:

1. Load the read diagnostic program in order to read cards while making the adjustment.
2. Display sync internal. A-B1K3B03 (XR301).
3. Adjust potentiometer (upper potentiometer) on the card, A-B1K3 as specified on AD000.

4.9.1.2 Punch Gate Single Shot

Objective: Provide a delay gate to allow the 1442 to accept punch data.

Adjustment:

1. Load the punch diagnostic program in order to punch cards while making the adjustments.
2. Display the output of the single shot, sync internal, A-B1K3B07 (XR301).
3. Adjust lower potentiometer on the card, A-B1K3 as specified on AD000.

4.9.2 1442 Card Read Punch Adjustments

The *Field Engineering Maintenance Manual, 1442 Card Read Punch, Models 6 and 7,* describes maintenance procedures for the IBM 1442 Card Read Punch.

4.10 PAPER TAPE DEVICES

4.10.1 Paper Tape Attachment Adjustments

4.10.1.1 Paper Tape Reader Single Shot

Objective: Set timing for transfer of information to the attachment.

Adjustment:

1. Load the paper tape reader program.
2. Sync oscilloscope minus internal on single-shot output on board A-B1G6B07 (XT301).
3. The adjustable potentiometer is the lower of the two on the card (toward card row 7).
4. Adjust single-shot output as specified on AD000.

4.10.1.2 1055 and 1134 Attachment Oscillator

Symmetry: Adjust the plus oscillator FF (AB1K6) (bottom potentiometer) (XT331) for 4.5 (±0.5) millisecond duration. Observe at AB1H7B09. Refer to AD000.

Frequency: Adjust the plus oscillator FF (AB1K6) (top potentiometer) (XT331) for 8.3 (±0.25) milliseconds between pulses. Observe at A-B147809. Refer to AD000.

4.10.1.3 Paper Tape Punch Attachment

See 4.10.1.2 for oscillator adjustment. There are no adjustments on the punch portion of the paper tape attachment.

4.10.2 1134 Paper Tape Reader Adjustments

The *Field Engineering Instruction Maintenance Manual, 1134 Paper Tape Reader,* describes maintenance procedures for the IBM 1134 Paper Tape Reader.

4.10.3 1055 Paper Tape Punch Adjustments

The *Field Engineering Maintenance Manual, 1054/1055 Paper Tape Reader/Punch,* describes maintenance procedures for the IBM 1055 Paper Tape Punch.

4.11 1132 PRINTER

4.11.1 1132 Printer Attachment Adjustments

4.11.1.1 CB Single Shot

Adjust this single shot as spccified on AD000.

4.11.2 1132 Printer Adjustments

The *Field Engineering Maintenance Manual, 1132 Printer,* describes maintenance procedures for the IBM 1132 Printer.

4.12 1627 PLOTTER

4.12.1 1627 Plotter Attachment Adjustments

Adjust the 1627 single shots as specified on logic AD000.

Note: Attachment contains jumpers that are changed for Model 1 and Model 2. Refer to AD000.

4.12.2 1627 Plotter Adjustments

The *Field Enginering Maintenance Manual, 1627 Plotter,* describes maintenance procedures for the IBM 1627 Plotter.

4.13 STORAGE ACCESS CHANNEL

This test procedure assumes that an I/O device is installed on the SAC and all signals are properly terminated.

The levels are standard SLT. The up levels are dependent on customer termination voltage for the twisted pair cable.

Signal scoping should be performed on the SLT connector specified at the output of the driving block.

4.13.1 CPU to SAC Signal Checkout

4.13.1.1 Channel Data Out Bits 0-15 (FA111, FA121)

1. The channel data out bits reflect the contents of the SBR at all times. These lines can be checked by loading the SBR with 0000 and scoping the line(s) in question. Next, load the SBR with FFFF and determine if the proper level exists by scoping.

Note: Instead of scoping it is possible to use the CE Indicators on the console.

2. **Additional checks can be made on a dynamic basis** by loading in the following program. Address 0002 may be loaded with desired bit pattern.

```
0000   C001   Start   LD    Load
0001   6000           LDX   Start
0002   XXXX   Load    DC
```

Set the console mode switch to run position and execute. Scope to ensure that channel data out lines have pulses on them.

4.13.1.2 Channel Reset (FA101)

Place scope on channel reset B-B1M7B12 and depress the reset pushbutton. The line level should go from +3v to approximately 0 volts when the pushbutton is depressed.

4.13.1.3 CPU Clock (FA101)

Load the program called out in paragraph 4.13.1.1-2. With program running check T clocks.

4.13.1.4 Phase A (FA101)

With CPU power applied scope line.

4.13.1.5 CS Level 1 and CS Clocks (FA101)

1. To cause a CS level 1
   a. Press IMM stop pushbutton.
   b. Press reset pushbutton.
   c. Place console mode switch to SS position.
   d. Request CS level 1 by jumpering B-A1F7D05 to ground. (See KM 211)

Note: Run trigger will not be on but X7 will go out when CPU is cycle stealing. If reset pushbutton is pressed while jumper is applied, parity checks may result.

2. CS Level 1 (FA101)
   a. Place console Mode Switch to SMC. The CPU will commence cycle stealing. Scope CS Level 1 line (B-B1M7D12) to see that it is activated.
   b. Press IMM stop pushbutton.
   c. Remove jumper B-A1F7D05 to ground.

4.13.1.6 XIO E-1 Cycle (FA101)

1. Load following bit switch program and execute:

0000	0801	XIO	Init. XIO Operation
0001	6000	LDX	Load IAR to zero
0002	0003	DC	
0003	0000	DC	

2. Scope XIO E-1 (B-A1N6D07) cycle line at SLT connector. Machine will be in two instruction loops:

   XIO instruction takes I1, E1, E2, E3 cycles.
   LDX instruction takes I1 cycle.

4.13.1.7 CPU Run (FA181)

1. Clear core to 0000.
2. Place console mode switch to the run position.
3. Press program start pushbutton switch.
4. CPU run line will be activated for approximately 400 ms.

4.13.1.8 CPU Parity Stop (FA181)

1. Refer to KR111 for source of parity stop.
2. Jumper B-A1J3D05 to B-A1J3D08.
3. Scope line at SLT connector with and without jumper.
4. Remove jumper from B-A1J3D05 to B-A1J3D08.

4.13.1.9 Channel Interrupt Levels (FA111, FA121)

The following procedure is for interrupt level 2. The remaining interrupt levels (3, 4, and 5) can be checked out in a similar manner.

1. Load the following core locations:

0000	3000	W
000A	000E	DC Transfer Vector Level 2
000B	000E	DC Transfer Vector Level 3
000C	000E	DC Transfer Vector Level 4
000D	000E	DC Transfer Vector Level 5
000E	0000	DC Transfer Vector
000F	4C400000	BOSC Reset Interrupt

2. Place console mode switch in the run position.
3. Jumper B-A1C7B02 to B-A1C7D08 (See FA181). Be sure that ground is applied at the output of 3813 to prevent damaging customer I/O drivers.
4. CPU will run in two instruction loops:
   a. Forced BSI due to interrupt request.
   b. Execute BOSC, resetting highest interrupt level in progress, which in this case is interrupt level 2.
5. Scope interrupt level 2 (FA111 levels 2, 3 – FA121 levels 4, 5)
6. Remove jumper from B-A1C7B02 to B-A1C7D08.
7. Follow same procedure for interrupt levels 3 through 5.

B-A1C7D02	For Level 3
B-A1C7B03	For Level 4
B-A1C7D05	For Level 5

4.13.2 SAC to CPU Signal Checkout

Disconnect cable from I/O device to SAC. All jumpers added to change line states should be placed on SLT connectors from twisted pair cable. This insures that the maximum portion of the net is checked.

4.13.2.1 Channel Write Gate (FA181)

1. Connect B-B1A7B13 to B-B1A7D08.
2. Turn off all bit switches.
3. Place console mode switch to load position.
4. The SBR should contain FFFF because channel data in bits are in true state. If SBR is blank, channel write gate logic is faulty. If one or two bits are missing, this could be caused by faulty terminator card or bad connection.
5. Remove jumper from B-B1A7B13 to B-B1A7D08.

4.13.2.2 Channel Data in Bits 0-15 (FA151, FA161)

1. For a static check perform 4.13.2.1 steps 1, 2, and 3. The absence of a bit in the SBR may be caused by jumpering the channel data in lines to ground at the SLT connector that is specified at the input to the 7196 terminator card.
2. For dynamic check load the following program:

0000	0803	Start	XIO	RD
0001	C004		LD	RDCHR
0002	18D0		RTE	16
0003	600C		LDX	Start
0004	0006	RD	DC	6
0005	0200		DC	1200
0006	0000	RDCHR	DC	0

   a. Place jumper on channel write gate as in paragraph 4.13.2.1, step 1.

b. Place console mode switch in run position. Accumulator extension (Q register) reflects the contents of the I/O input bus. Pattern in Q register may be altered by jumpering channel data in lines to ground at the SLT connector that is specified at the input to the 7196 terminator card.
c. Remove jumpers.

4.13.2.3 Channel CS Register Level 1 (FA181)

1. Press IMM stop pushbutton.
2. Press reset pushbutton.
3. Place console mode switch to SS position.
4. Request CS level 1 by jumpering B-B1A7D13 to ground.
5. Place console mode switch to SMC position. The CPU should be cycle stealing. The run light does not come on, but X7 light is extinguished. If reset pushbutton pressed while jumper is applied, a parity check may result.
6. Remove jumper.

4.13.2.4 Storage Address Bits (FA131, FA141)

1. Perform procedures 4.13.2.3 steps 1 through 5. The core storage is addressed by the SAC terminating cards during CS level 1. With no jumpers connected to storage address bits, the highest address in core storage is read and displayed in the SBR.
2. The storage address bits can be tested by alternately grounding them at the SLT connectors, and using the data stored in that particular core location as the indication of proper addressing.
3. Remove jumpers.

4.13.2.5 Block Clock Advance

1. Perform procedures 4.13.2.3 steps 1 through 5.
2. Press IMM stop pushbutton.
3. Turn console mode switch to SS position. Press program start twice, X clock advances to X1.
4. Place jumper on B-B1A7D12 to B1A7D08.
5. Depress program start six times, X7 light should remain off and X clock should remain at X1. Verify that X1 is still on by scoping B-A1D5D12. (See KM101).
6. Remove block clock advance jumper B-B1A7D12 to B-B1A7D08.
7. Press program start six times the X7 light should be lit.
8. Replace B-B1A7D12 to B-B1A7D08.
9. Now press program start several times. X7 light should remain lit.
10. If step 5 or step 9 fail, scope the block clock advance net for missing line or bad module.
11. Remove jumpers.

4.13.2.6 Channel Interrupt Request 2 Through 5 (FA121)

1. Perform 4.13.1.9 steps 1 and 2.
2. Jumper interrupt level 2 request at SLT connector B-A1N6B09 to ground. Press program start pushbutton.
3. Refer to 4.13.1.9 step 4. Check console display to verify that interrupt level 2 is on.
4. Remove jumper B-A1N6B09 to B-A1N6D08.
5. Follow similar procedure for interrupt requests 3, 4, and 5. SLT connectors are functioning properly.

4.14 SYNCHRONOUS COMMUNICATIONS ADAPTER

4.14.1 Transmit Timer Delay

Objective: Provide a timeout interrupt of 1.25 seconds after turning on the synchronize flip-flop.

Adjustment: Adjust the potentiometer on the time delay card as specified on AD000.

4.14.2 Receive Timer Delay

Objective: Provide a timeout interrupt of 3.0 seconds after entering receive mode.

Adjustment: Adjust the potentiometer on the time delay card (FC341) as specified on AD000.

4.14.3 Timeout Single Shot

Objective: Provides a reset to the three timers in the SCA. The timeout single shot is fired with any timeout signal, an XIO sense with reset (bit 14) instruction, or an 'all turnaround' signal.

Adjustment: Adjust the potentiometer on the single shot card (FC341) as specified on AD000.

4.14.4 Delay Single Shot

Objective: Fired when in receive mode and the end-op instruction is issued. This single shot keeps the SCA in a busy status and provides the data-set interface with the 'data terminal ready' line for one millisecond. 'Data terminal ready' is controlled by a jumper in the SCA. Refer to logic page FC331.

Adjustment: Adjust the potentiometer on the single shot card (FC741) as specified on AD000.

4.14.5 Program Timer

Objective: This timer causes a timeout interrupt in BSC mode only. This interrupt times the programmed insertion of the synchronous-idle sequence into the data stream.

Adjustment: Adjust the potentiometer on the time delay card (FC341) as specified on AD000.

4.14.6 CE Single Shot

Objective: This single shot inhibits SCA interrupts when the SCA is in CE mode and the CE mode switch is turned off. Turning this switch off fires the single shot causing a reset to the SCA. It is during this reset that interrupts must be prevented to allow off-line servicing.

Adjustment: Adjust the potentiometer on the single shot card (FC331) as specified on AD000.

4.14.7 Receive Shift Single Shot

Objective: Fired with 'receive shift' trigger. This single shot provides the shift pulse for the 'receive deserializer', and also provides the proper timed pulse for clock correction.

Adjustment: Adjust the potentiometer on the single shot card (FC361) as specified on AD000.

4.15 2501 CARD READER

4.15.1 2501 Attachment Adjustments

Adjust the Erase Check and the Record Emitter single shots as specified on AD000.

4.15.2 2501 Card Reader Adjustments

The *Field Engineering Maintenance Manual, 2501 Card Reader,* describes maintenance procedures for the IBM 2501 Card Reader.

4.16 1231 OPTICAL MARK PAGE READER

4.16.1 1231 Attachment Adjustments

Adjust the Select and the Timing Mark single shots as specified on AD000.

4.16.2 1231 Optical Mark Page Reader Adjustments

The *Field Engineering Maintenance Manual, 1231 Optical Mark Page Reader,* describes maintenance procedures for the 1231 Optical Mark Page Reader.

4.17 1133 MULTIPLEXER

The *Field Engineering Theory-Maintenance Manual, 1133 Multiplexer Control,* describes maintenance procedures for the 1133 Multiplexer Control.

Section 1. Basic Machine

5.1 GENERAL INFORMATION

DANGER

Exercise extreme care when servicing or inspecting the power supply area. Dangerous voltages and currents are present even when the system is in a power-off status. If necessary to connect a test instrument within a power supply, or to reach into it for any reason, disconnect the mainline cord. Discharge capacitors before working near them. Each heat sink is at an electrical potential.

5.1.1 Power Distribution and Sequencing

Power supplies are highly reliable units. Individual troubles in these areas, therefore, usually result in high service time for that system. To control these high service time calls, certain basic hardware checking is provided (Figure 5-1).

5.1.2 Switches

Emergency Power Off: (not customer resettable). Turns off all primary transformer power in the processor, except the 24 vac power. Drops all power to I/O machines.

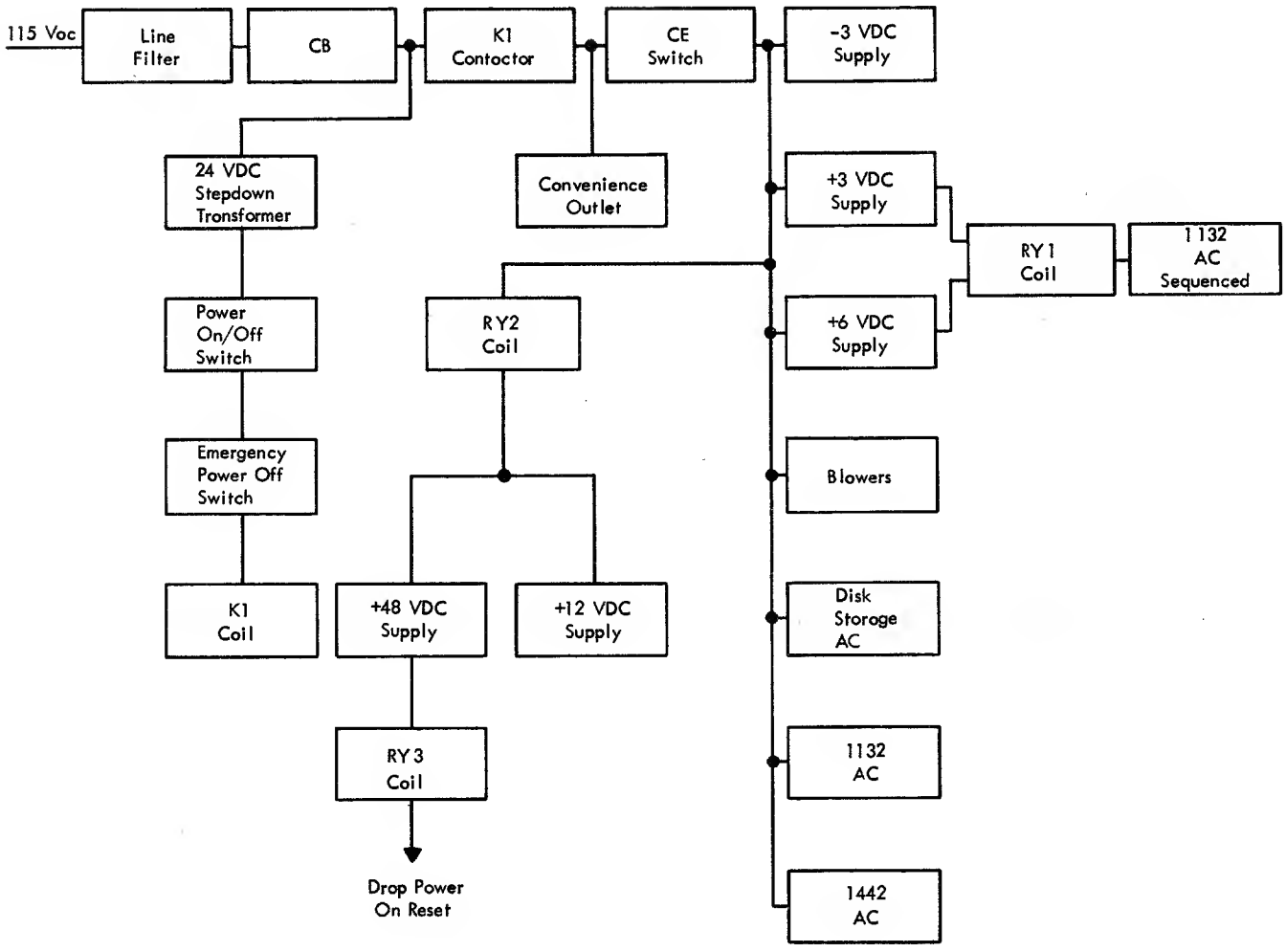


Figure 5-1. Voltage Distribution

Power On/Off: Same as emergency power off except resettable.

Disk On/Off: Controls ac power to the disk storage drive.

5.1.3 CE Power Switches

Processor: Removes all primary power to system except processor convenience outlets.

Printer: Removes primary power in printer. Removes power to motors except chassis cooling fans. Leaves convenience outlets on.

Reader Punch: Same functions as for printer.

5.1.4 Indicators

Ready: Indicates when power is up.

5.1.5 Voltage Variation

These voltages which can provide an indication of a deteriorating component condition can be varied within ±4% to assist in isolating extreme difficulties. See table in 5.1.9.

5.1.6 Convenience Outlet

A 115 vac convenience outlet is provided in the CPU. It is fused at 6.25 amps.

5.1.7 Voltages Present Under Normal Power Off Conditions

1. 24 vac circuits.
2. 115 vac in sequence box.

5.1.8 Input Power Specifications

60 Hertz: The IBM 1130 System operates from a 115v, or 208v/230v 60 hertz, single phase, three wire service line.

Input voltage may have a total variation of ±10% of the rated voltage. Line frequency must be 60 (±0.5) Hz.

The mainline CB is designed to trip when the input current is excessive. It must be reset manually.

50 Hertz: The 50 hertz version of the 1130 requires an input voltage of 195 vac, 220 vac, or 235 vac, single phase, three wire service line.

Input voltage may have a total variation of ±10% of the rated voltage. Line frequency must be 50 (±0.5) Hz.

5.1.9 Individual Power Supplies

Operating Limits: For normal operation, the dc power supplies must be maintained within the tolerances specified in the table below.

Voltage	Voltage Limits	Terminal
-3	- 2.88 to - 3.12	01A-TB1-6
+3	+ 2.88 to + 3.12	01A-TB2-9
+6	+ 5.76 to + 6.24	01A-TB1-9
+12	+ 11.16 to + 12.84	01A-TB2-17
+48	+ 44.16 to + 51.84	01A-TB2-18

The dc voltage tolerances include regulation and ripple.

5.1.10 Core Storage Voltages

Current Requirements:

Storage in Use	Storage Standby
+6v 4.0 amp	2.5 amp
+3v .6 amp	.4 amp
-3v 1.5 amp	.5 amp
+12v .5 amp	.0 amp

Voltage Limit: In order to prevent damage to the storage circuits, the supply voltages should never exceed -8.0v, +8.0v, +9.0v and +15v for -3, +3, +6, and +12 voltages, respectively. Transient voltages greater than 10% above nominal must be less than 50 milliseconds in duration. Undervoltage does not damage the storage.

Marginal Checking: There is no provision for marginal checking of storage voltages.

Power Sequencing: The special voltage, +12v, is applied to the storage large card after the SLT voltages have been established. It also is the first voltage to go down in case of failure of any SLT voltages (+6, +3, -3). The voltage +12 must be removed no more than 100 milliseconds after the failure.

Frequency Limits: The minimum period between the leading edges of a + read cycle and a + write cycle (and vice versa) is 1.75 microseconds. The minimum period for a full read/write cycle is 3.5 microseconds.

Adjustment: Adjustments for core storage voltage are covered in 4.2.

5.2 SERVICE CHECKS AND HINTS

1. All dc voltages should be within ±4%, including all noise and ac ripple, of their labeled values.
2. Loose wires at voltage distribution connectors can cause loss of or low voltage to the gates while the voltmeter indicates correctly.
3. A tripped power supply circuit breaker indicates a possible short in the output of the supply. Check the output for shorts to other supplies as well as to ground. These shorts are normally dead (near zero resistance) shorts. The minimum resistance to be expected can be determined by dividing the supply voltage by the maximum output current (E/I = R).
4. DC voltages should be measured at the SLT large boards.

5.3 CLEANING

The heat sinks must be clean to provide for heat dissipation and to prevent shorts.

5.4 ADJUSTMENTS AND REMOVAL PROCEDURE

5.4.1 Removal

1. Turn off the mainline switch. Remove the line cord. Bleed the capacitors.
2. Disconnect the leads to the particular supply to be removed.
3. Remove the holding clips on the power supply. Slide the supply forward and out of the machine (+3 must come out through the top).

5.4.2 Adjustments

For normal operation the DC power supplies must be adjusted within the tolerances specified in the following table.

Voltage	Voltage Limits	Terminal
-3	- 2.88 to - 3.12	01A-TB1-6
+3	+ 2.88 to + 3.12	01A-TB2-9
+6	+ 5.76 to + 6.24	01A-TB1-9
* +12	+ 11.16 to + 12.84	01A-TB2-17
* +48	+ 44.16 to + 51.84	01A-TB2-18

*Non-adjustable.

The dc voltage tolerances include regulation and ripple.

5.5 DIAGNOSTICS

If one or more circuit breakers trip to the off position when power is applied, check their outputs for shorts to other voltage levels, as well as to ground.

Note: A good ohmmeter that can peg to zero resistance on the R x 1 scale must be used because of the very low total resistance of the circuits. Look for dead shorts. The minimum resistance to be expected can be found by dividing the supply voltage by the maximum output current. If trouble is in an individual power supply, some of the following points may be useful:

1. On the logic diagrams, those parts enclosed within dotted or broken lines are located on the circuit cards or in the overvoltage device.
2. Series power supply transistors are those other than the ones on the power supply circuit cards.
3. With the power supply removed, 110 vac can be wired into TB pins (check diagrams). Output may not reach full value, but should be close and adjustable (remove overvoltage device or overvoltage circuit card).
4. Visually inspect the unit for crimped wires or cable chafing (unit may work in opened position, but not in a closed position).
5. If the voltage is too high and cannot be varied by the adjusting control, check for shorted series power supply transistors (located on the large power supply heat sink), or for a bad power supply circuit card.
6. If the output voltage is high and CB did not trip, replace the overvoltage protective device or overvoltage card (if supply is so equipped).

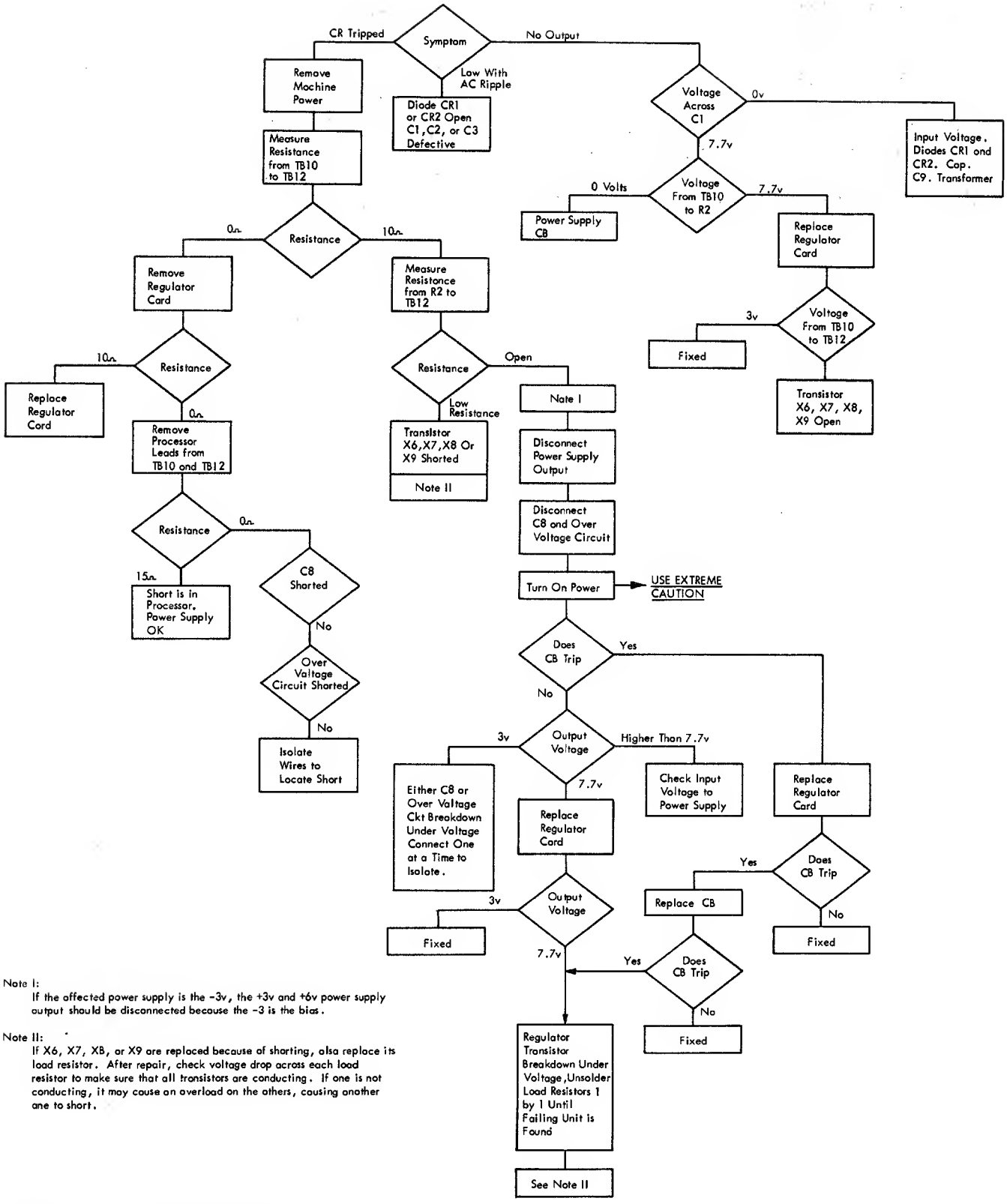
7. An open diode in the rectifier circuit shows up as low voltage under load. This can be detected by feeling the diodes: they are quite warm when operating normally. If one is cold, it is probably open.
8. A shorted diode in the rectifier circuit should trip the circuit breaker in the primary of the input transformer. It may also trip the overcurrent CB because of overvoltage spikes on the output. With the overvoltage device removed, the spikes can be scoped at the output terminals.
9. Shorted or open series power supply transistors can be detected by scoping or by checking the resistors in the emitter circuit for heat.
10. Check voltages after the machine has been on for 15 minutes. Voltage may drift slightly between cold and warm states.
11. Do not ground the meter or scope to the heat sink. Instead, ground to the holding screws at the corners of the unit.
12. If the system powers down immediately after a power up and the voltage of the various power supplies are correct, remove the overvoltage device from the power supplies one at a time and repeat the power up sequence. If power up is successful, the power supply voltage is wrong or the overvoltage device is faulty.

5.5.1 MPS Power Supply Trouble Symptom Analysis Chart

Analysis techniques for the +3v, -3v, +6v supplies are the same even though some of the components are different. The 3v supply (YP003) was used for this chart (Figure 5-2).

Note 1: If the affected power supply is the -3v, the +3v and +6v power supply output should be disconnected because the -3v is the bias.

Note 2: If X6, X7, X8, or X9 is replaced because of shorting, replace its load resistor also. After repair, check voltage drop across each load resistor to make sure that all transistors are conducting. If one is not conducting, it may cause an overload on the others, causing another one to short.



Note I:
If the affected power supply is the -3v, the +3v and +6v power supply output should be disconnected because the -3 is the bias.

Note II:
If X6, X7, X8, or X9 are replaced because of shorting, also replace its load resistor. After repair, check voltage drop across each load resistor to make sure that all transistors are conducting. If one is not conducting, it may cause an overload on the others, causing another one to short.

Figure 5-2. MPS Power Supply Flow Chart

5.6 -12v SUPPLY FOR SCA

A special -12v power supply is mounted on the added logic gate (01CA1) when the SCA feature is installed.

The -12v supply draws power from the +12 vac transformer.

The -12v supply is not adjustable. It measures -12v ±0.84v.

The -12v is supplied to the SCA oscillators and the converter (CV) circuits. These circuits convert data set voltage levels to SLT levels or vice versa.

The +12v and -12v service nets are shown on logic page FC221.

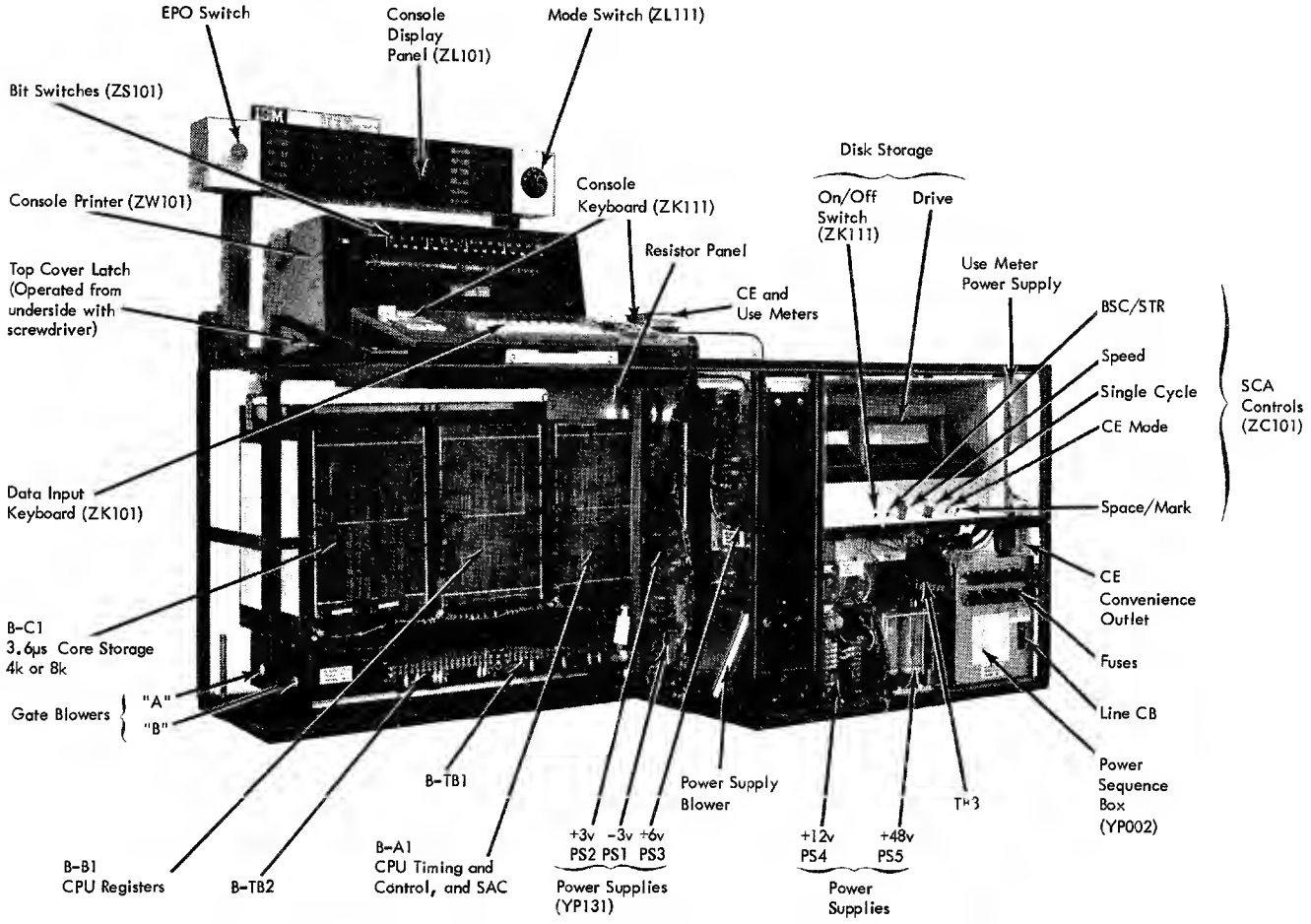


Figure 6-1. 1131 Central Processing Unit with MPS Power Supplies: View from Left Front

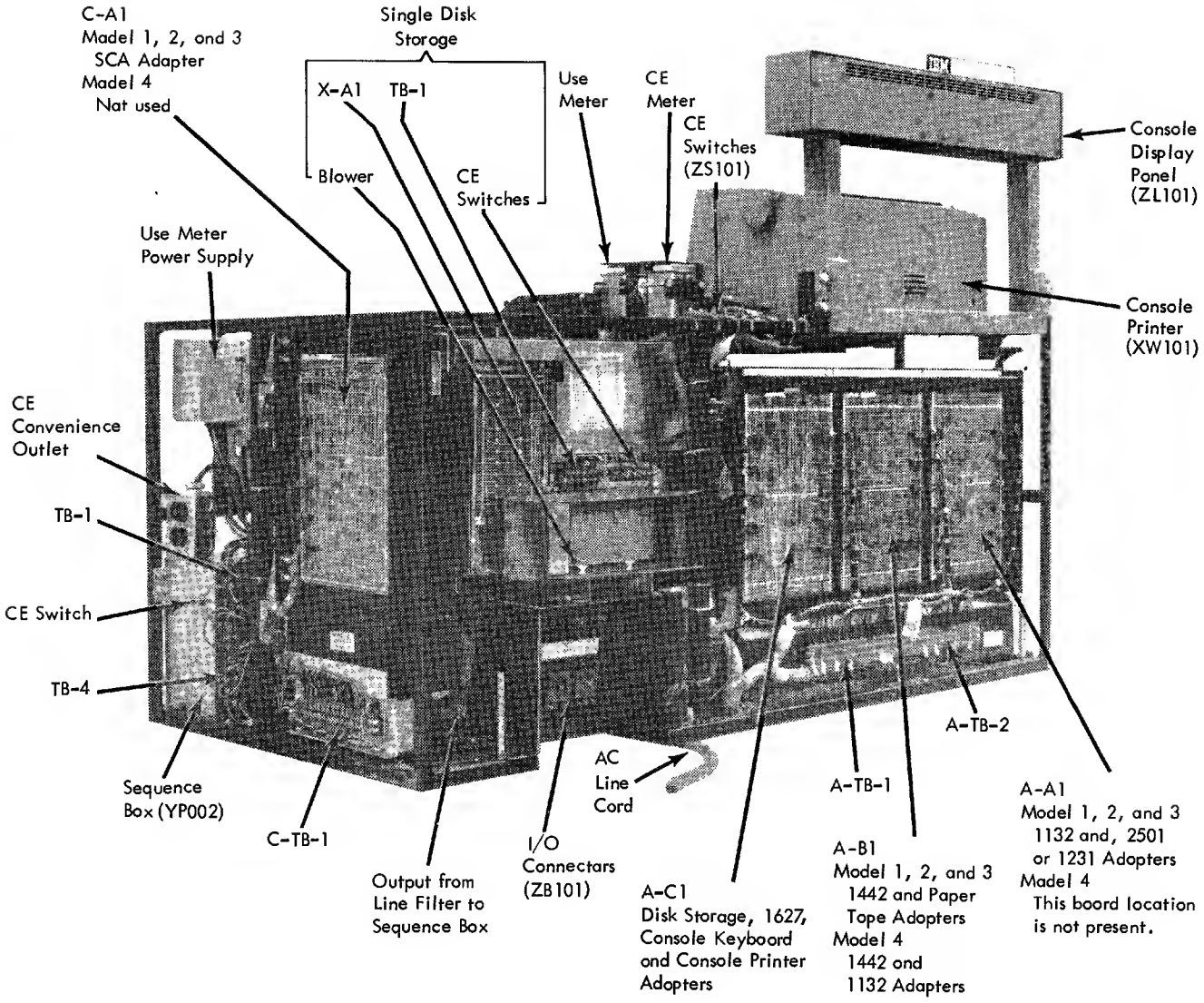


Figure 6-2. 1131 Central Processing Unit with MPS Power Supplies: View from Right Rear

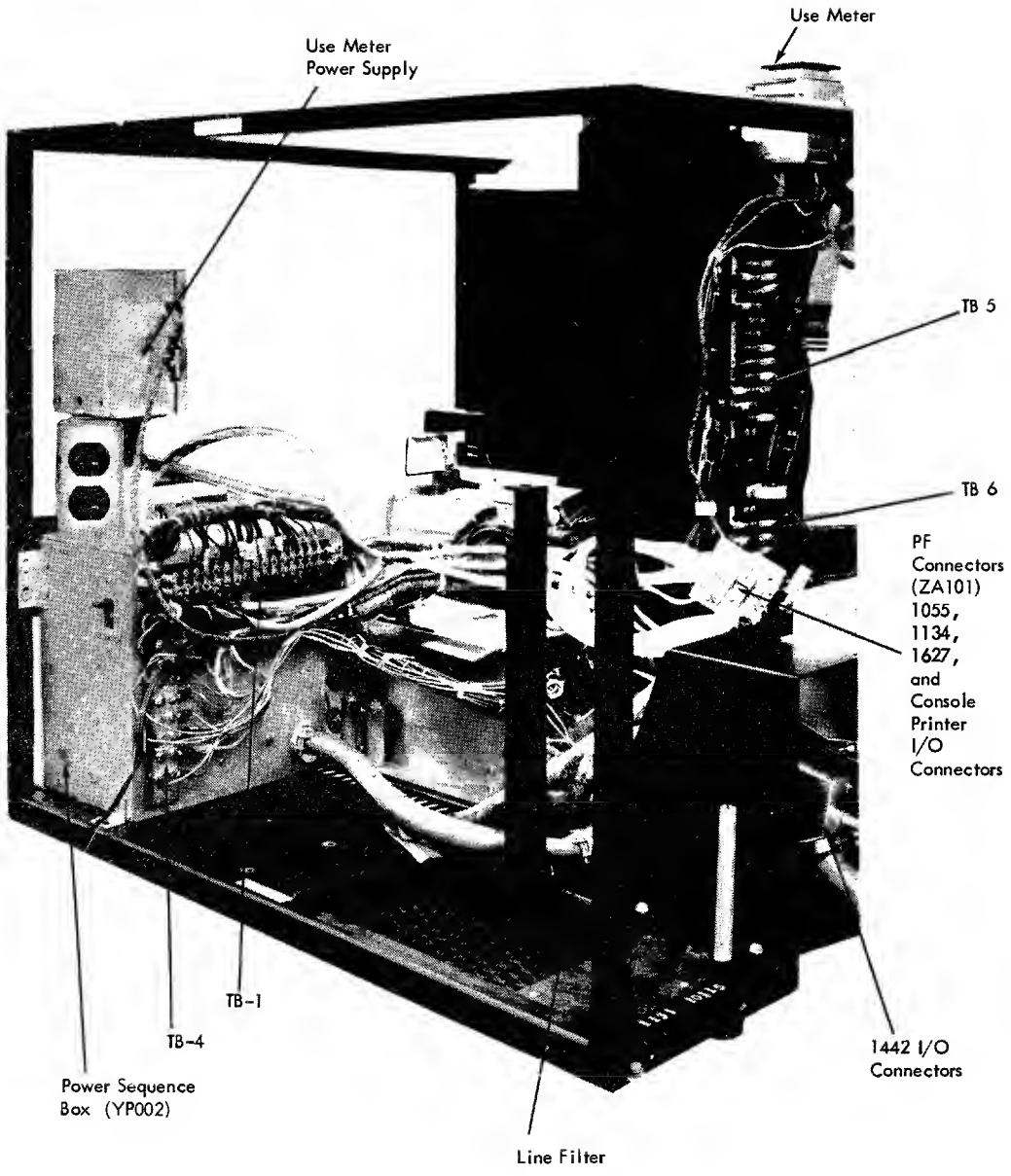


Figure 6-3. 1131 Central Processing Unit with MPS Power Supplies: I/O Connectors

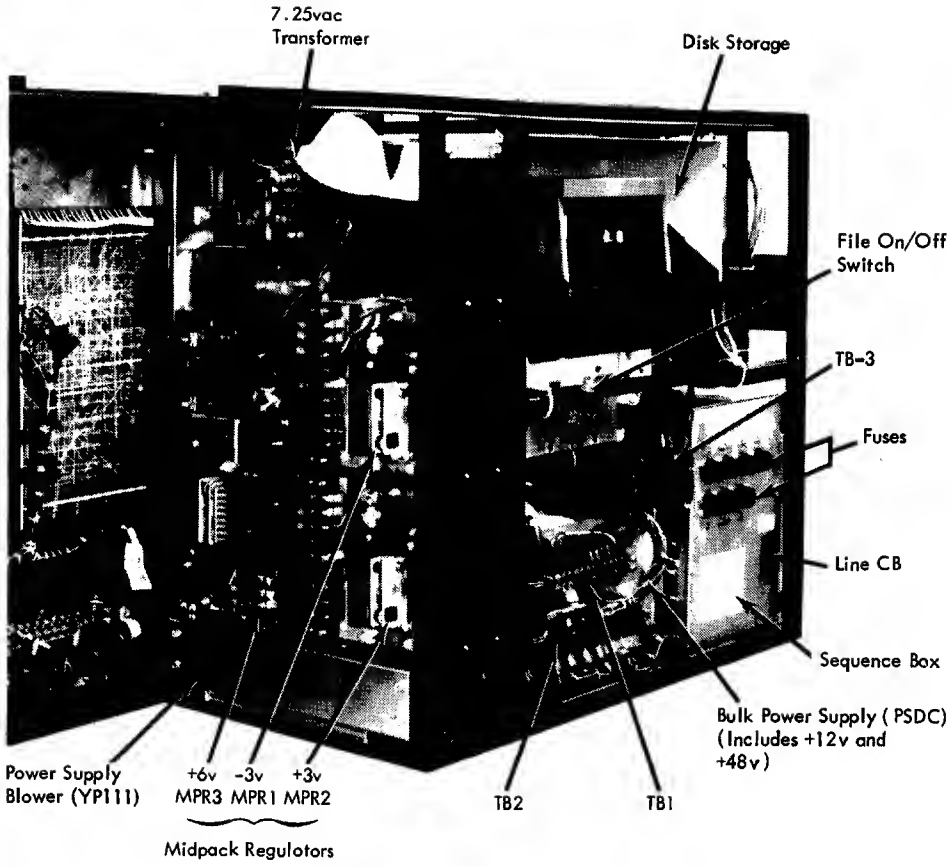


Figure 6-4. 1131 Central Processing Unit with Midpack Power Supplies: View from Left Front

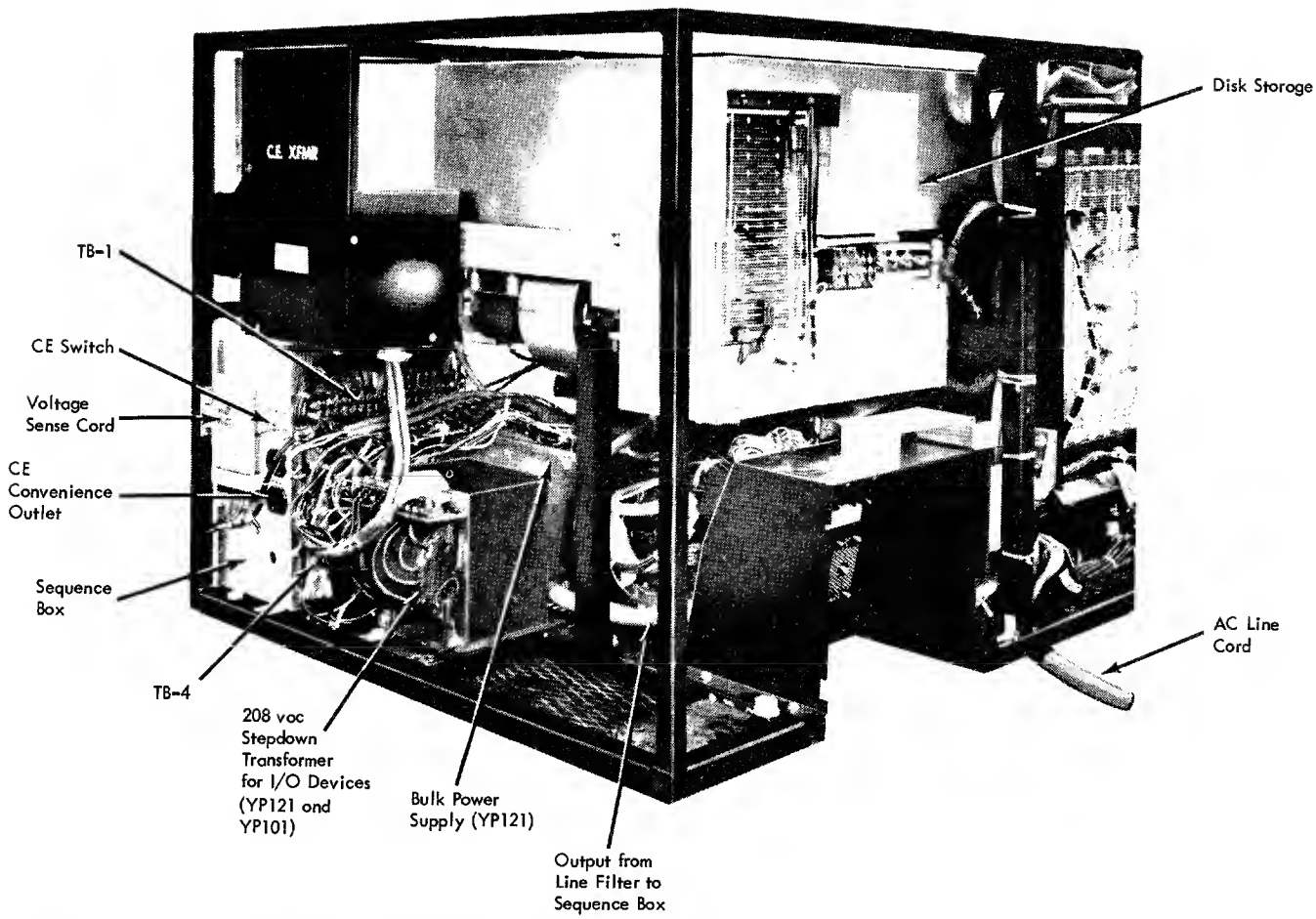
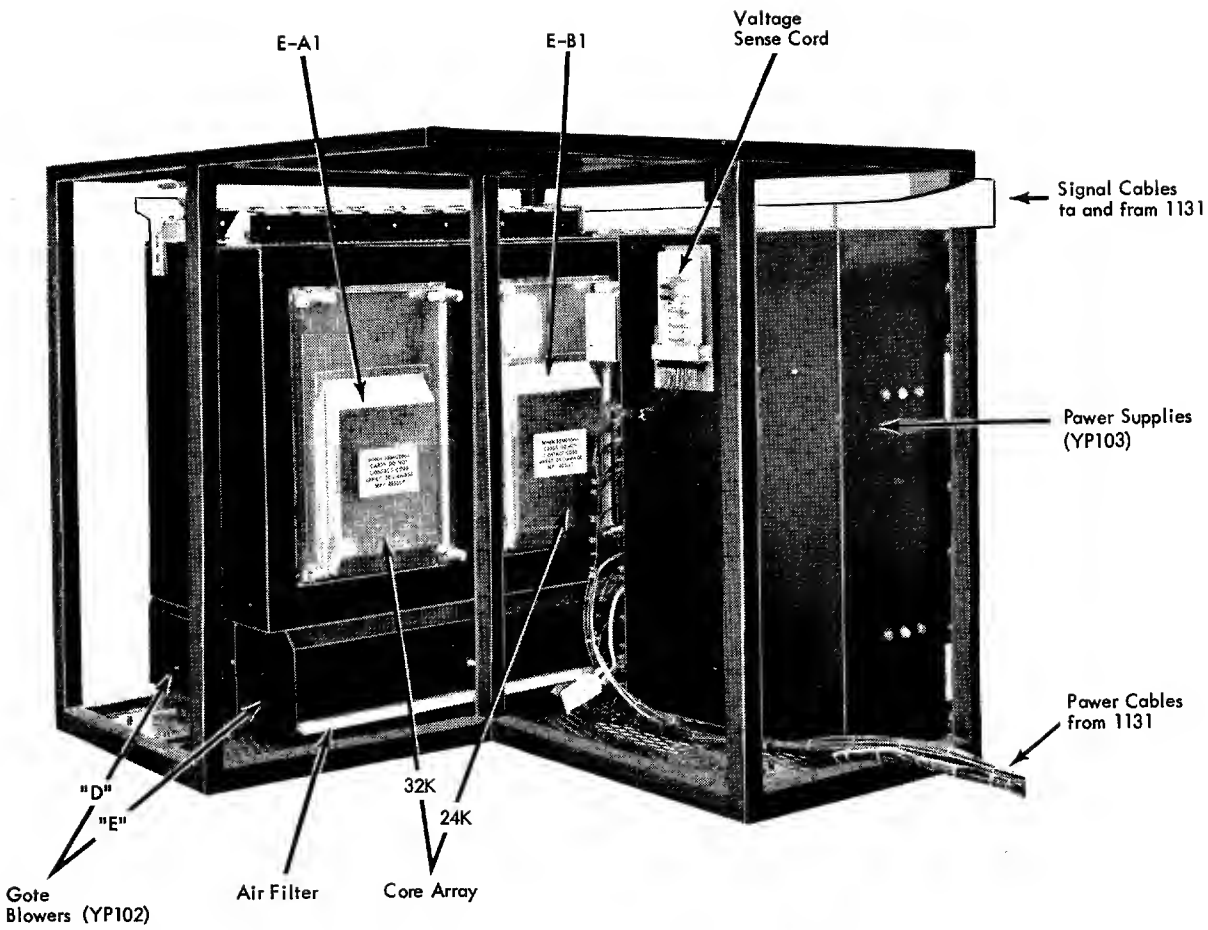
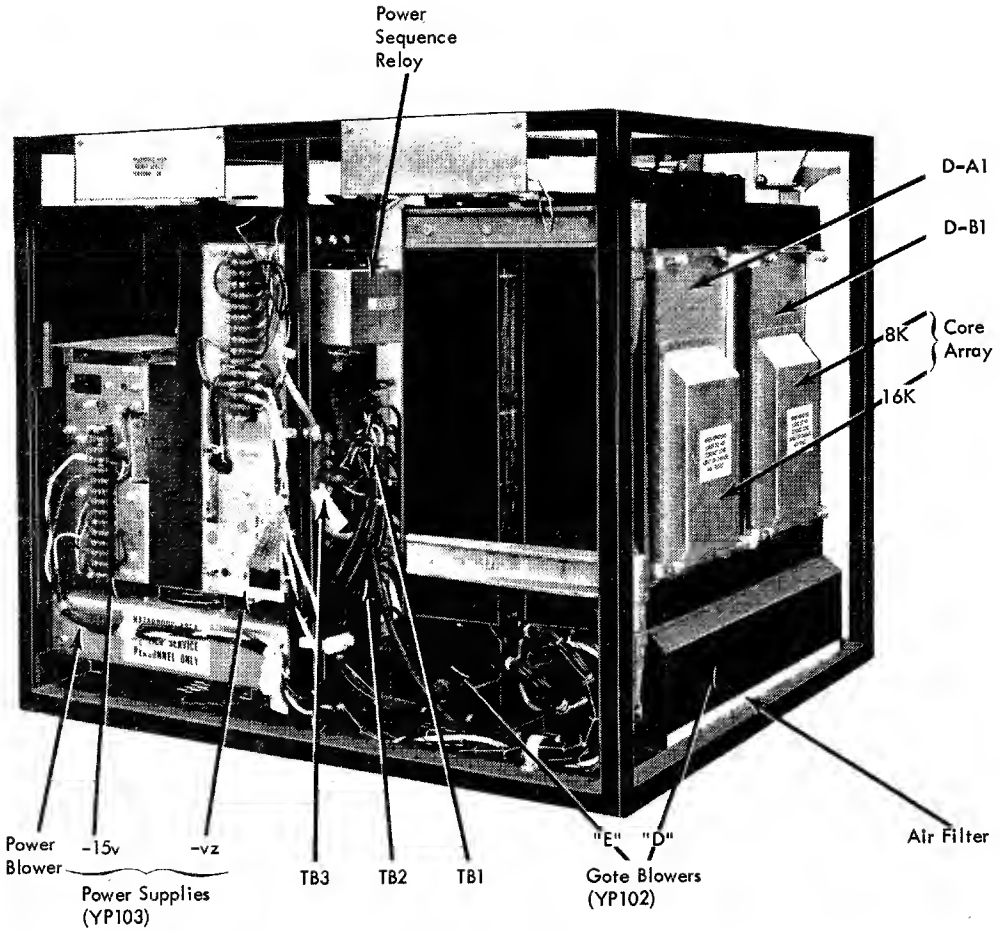


Figure 6-5. 1131 Central Processing Unit with Midpack Power Supplies: View from Right Rear



Nate: Refer to logic page YP009.

Figure 6-6. Core Storage Blister for 1131 Models 1C, 1D, 2C, 2D, 3B, 3C, 3D, 5B, 5C, and 5D: View from Right Front



Note: Refer to logic page YP009.

Figure 6-7. Core Storage Blister for 1131 Models 1C, 1D, 2C, 2D, 3B, 3C, 3D, 5B, 5C, and 5D: View from Left Rear (Model 3D Illustrated)

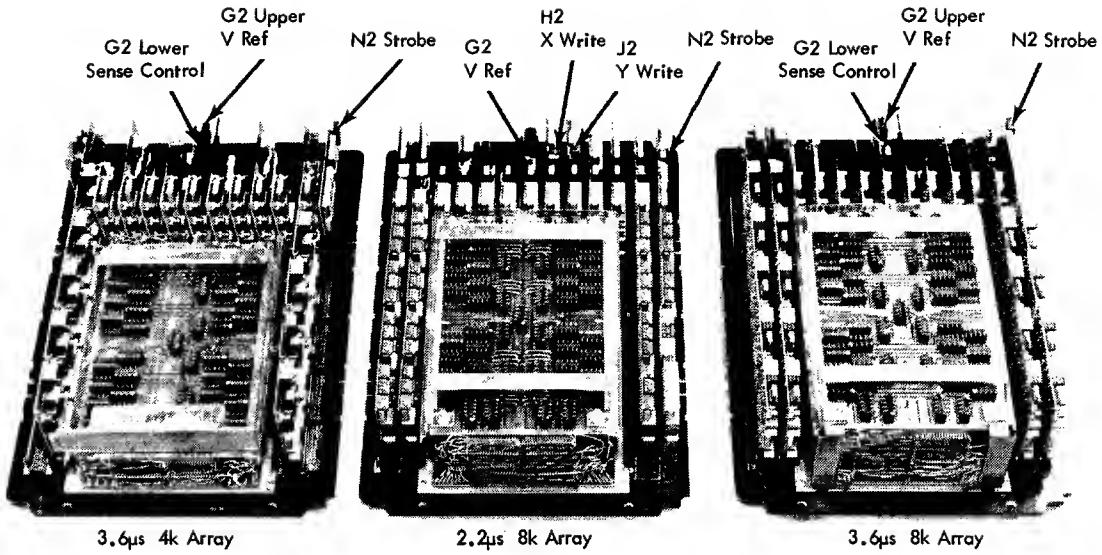


Figure 6-8. Core Storage Arrays

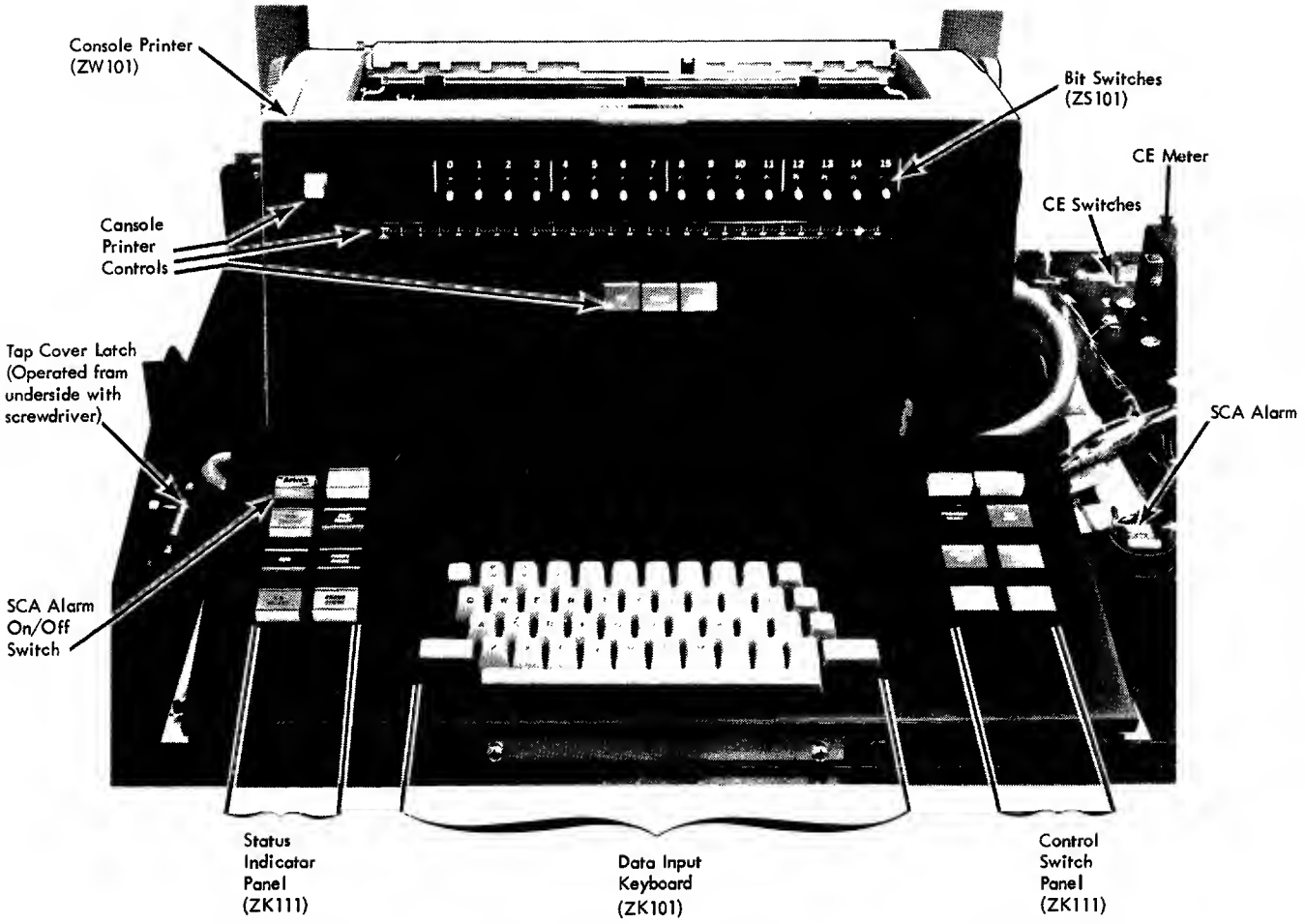
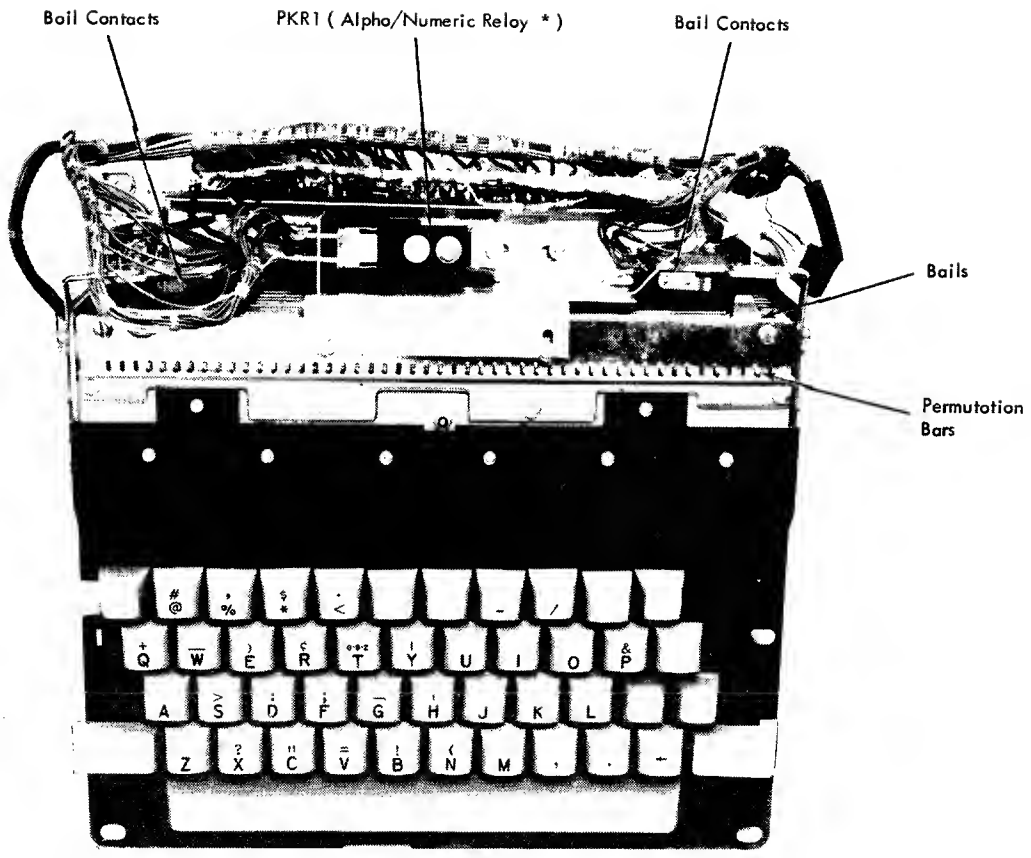
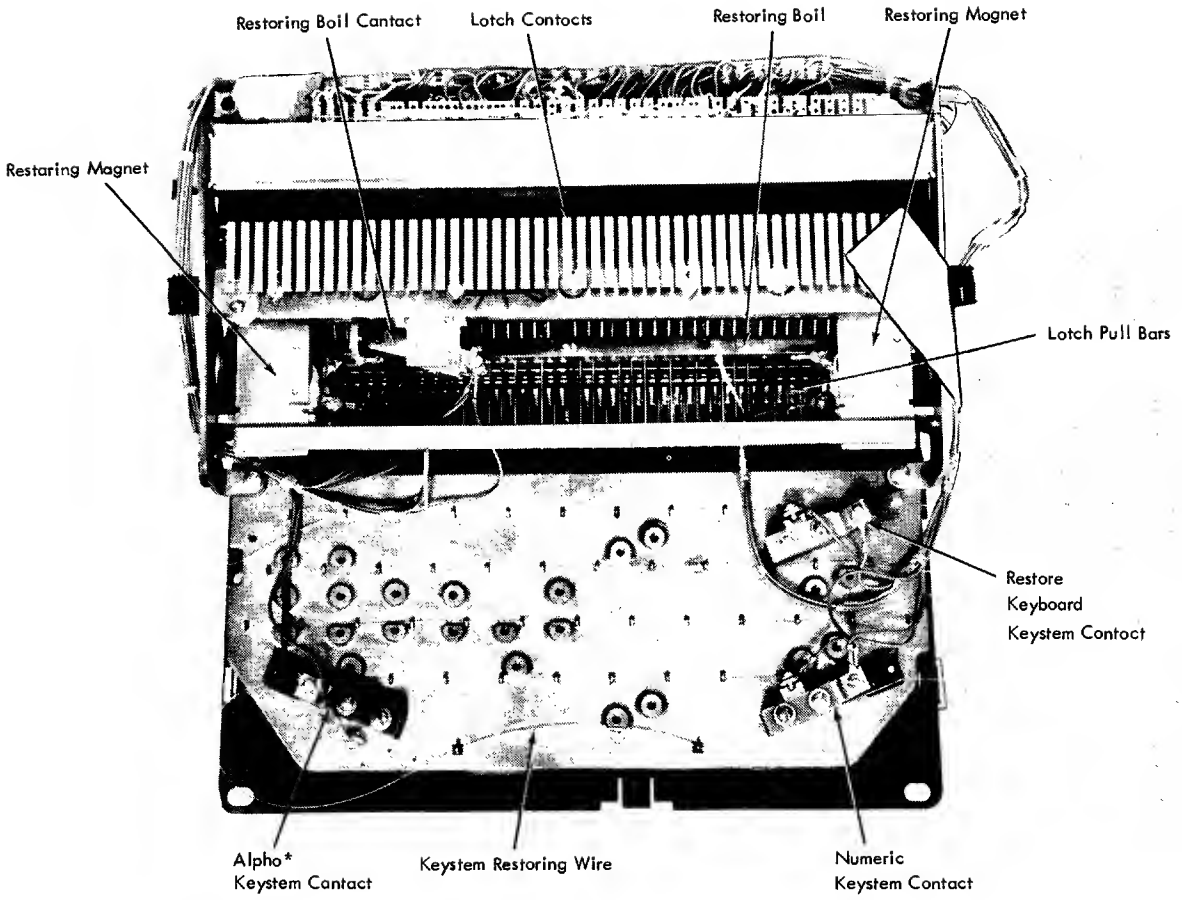


Figure 6-9. Console Printer and Keyboard



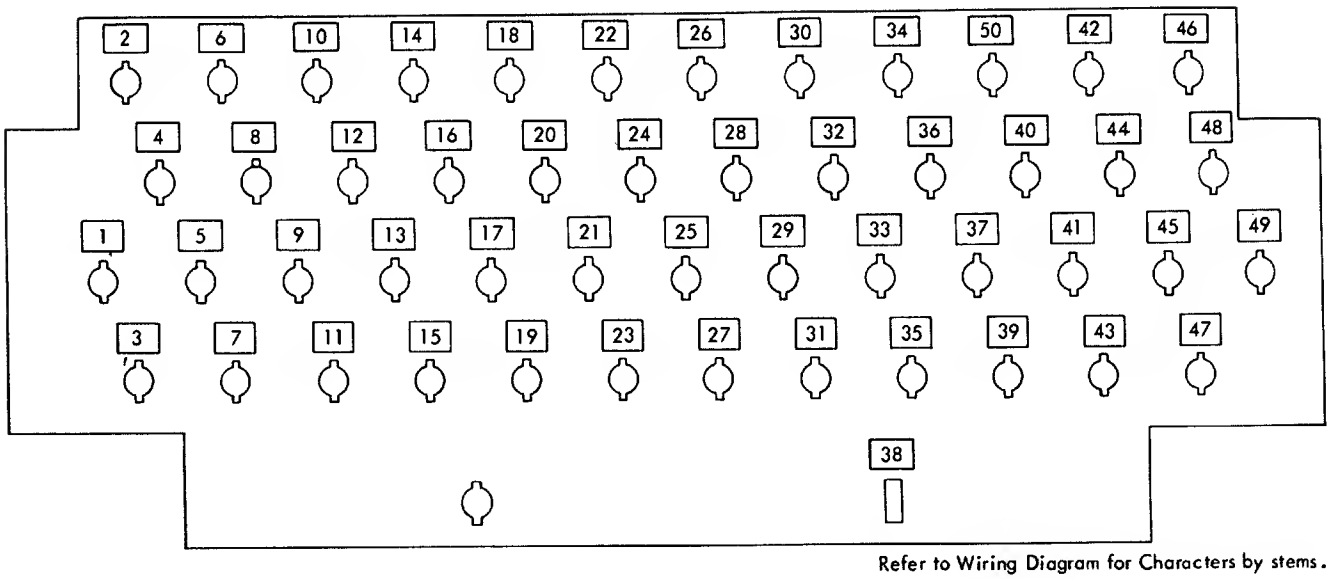
* Used only when Alpha key is installed.
Note: Refer to logic page ZK101.

Figure 6-10. Keyboard: Top View



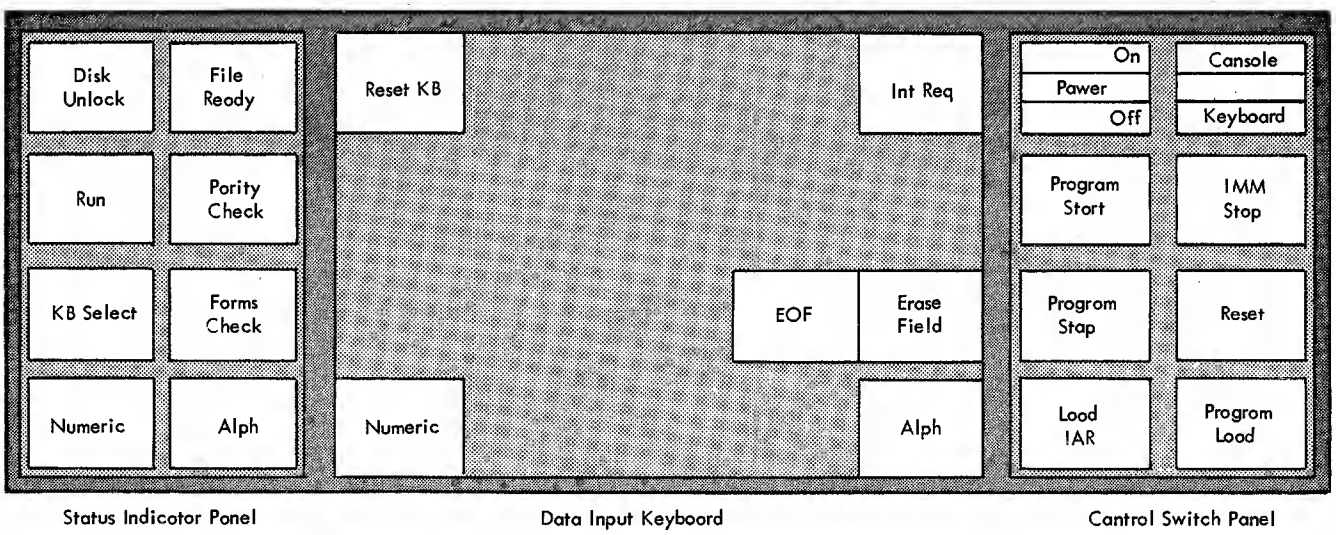
* Used only when Alpha key is installed.
Note: Refer ta logic page ZK121.

Figure 6-11. Keyboard: Bottom View

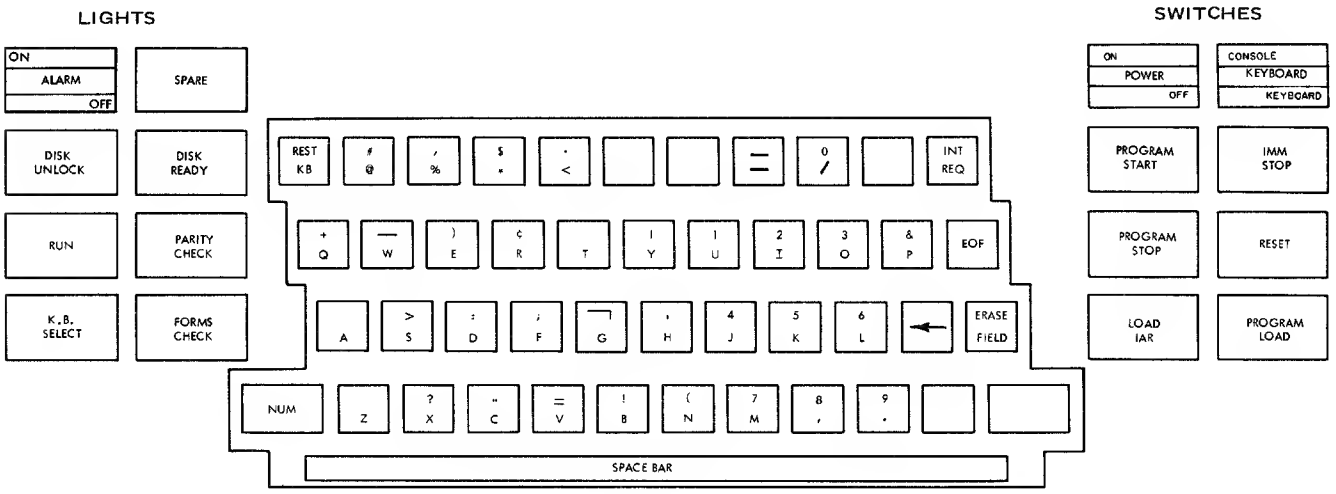


Refer to Wiring Diagram for Characters by stems.

Figure 6-12. Keyboard Keystem Numbering

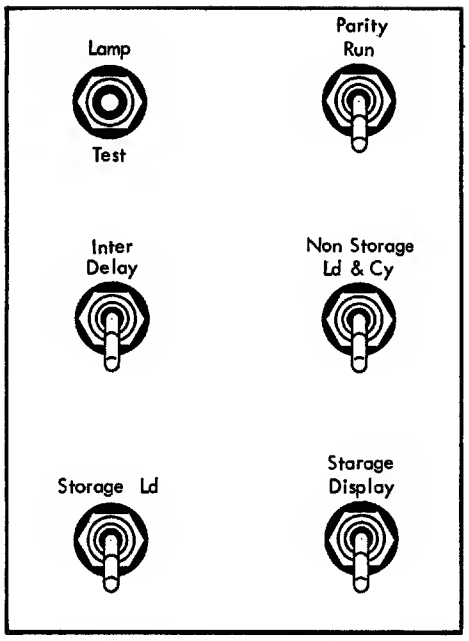


A. Machines with Serial Numbers below 11674 which do not have SCA.

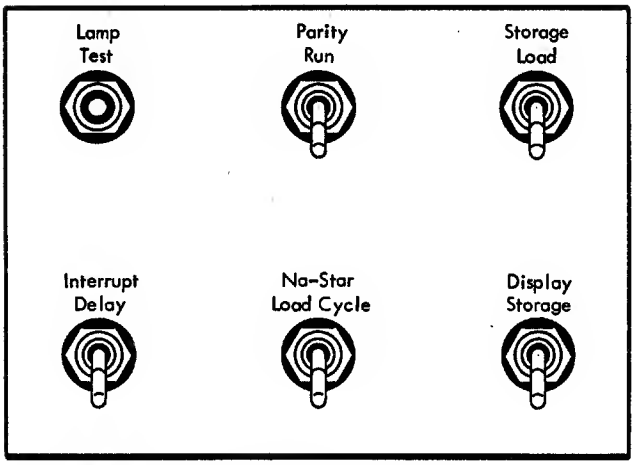


B. Machines with SCA or Serial Number 11674 and up

Figure 6-13. Console Keyboard.

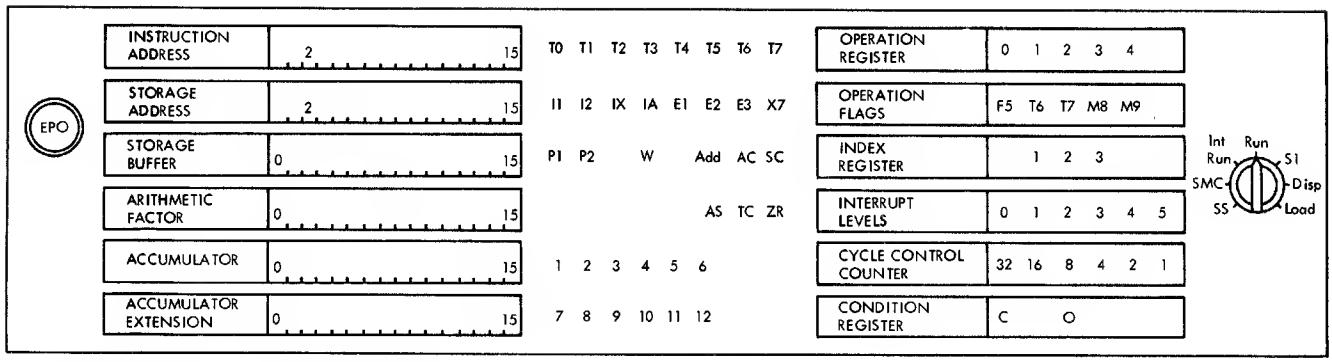


A. Machines with Serial Numbers 11477 or Lower.

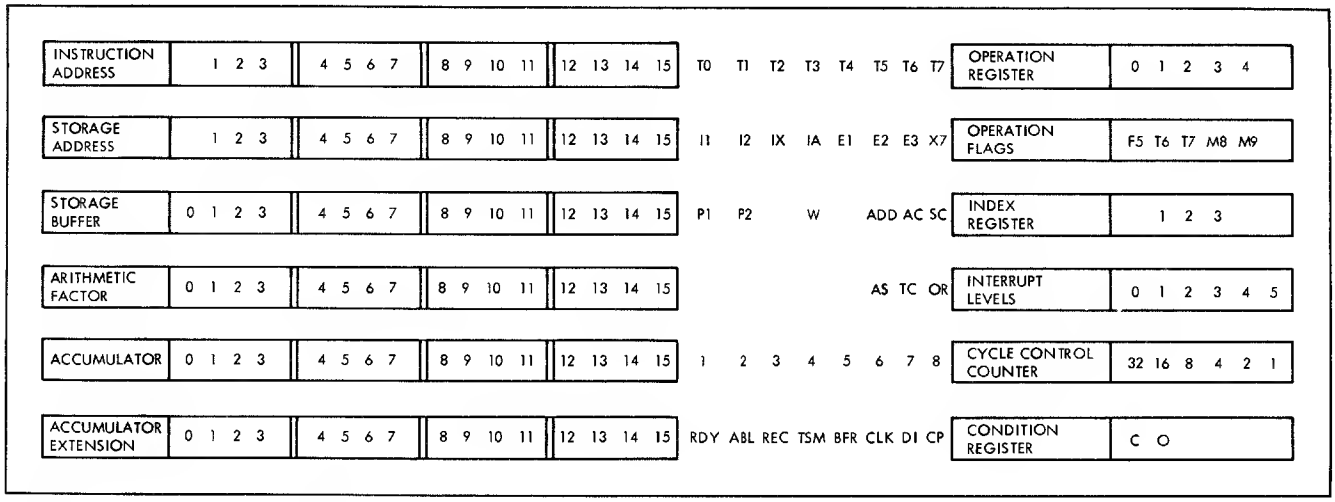


B. Machines with Serial Numbers 11478 and Up.

Figure 6-14. CE Panel



A. Machines with Serial Numbers below 11601 and without SCA.



8. Machines with SCA or Serial Numbers 11602 and up.

Figure 6-15. Console Display Panel.

Intentionally Blank

Where more than one page reference is given, the major reference is first.

IBM 1130 Computing System
Field Engineering Maintenance Manual
SY26-5977-5

READER'S COMMENT FORM

Your views about this publication may help improve its usefulness; this form will be sent to the author's department for appropriate action. Using this form to request system assistance or additional publications will delay response, however. ***For more direct handling of such requests, please contact your IBM representative or the IBM Branch Office serving your locality.***

Possible topics for comment are:

Clarity Accuracy Completeness Organization Index Figures Examples Legibility

Cut or Fold Along Line

What is your occupation? _____

Number of latest Technical Newsletter (if any) concerning this publication: _____

Please indicate your name and address in the space below if you wish a reply.

_____

_____

_____

Thank you for your cooperation. No postage stamp necessary if mailed in the U.S.A. (Elsewhere, an IBM office or representative will be happy to forward your comments.)

Your comments, please . . .

This manual is part of a library that serves as a reference source for systems analysts, programmers, and operators of IBM systems. Your comments on the other side of this form will be carefully reviewed by the persons responsible for writing and publishing this material. **All comments and suggestions become the property of IBM.**

Cut Along Line

Fold Fold

First Class
Permit 40
Armonk
New York

Business Reply Mail
No postage stamp necessary if mailed in the U.S.A.

IBM Corporation
Systems Publications, Dept 27T
P.O. Box 1328
Boca Raton, Florida 33432

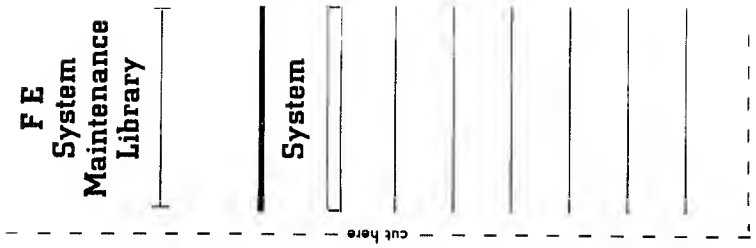
Fold Fold

1130 Computing System (FEMM) Printed in U.S.A. SY26-5977-5

IBM

International Business Machines Corporation
Data Processing Division
1133 Westchester Avenue, White Plaine, New York 10604
[U.S.A. only]

IBM World Trade Corporation
821 United Nations Plaza, New York, New York 10017
[International]



SY26-5977-5

IBM

International Business Machines Corporation
Data Processing Division
1133 Westchester Avenue, White Plains, New York 10604
[U.S.A. only]

IBM World Trade Corporation
821 United Nations Plaza, New York, New York 10017
[International]